Application

- Digital oscilloscopes
- Communication receiver
- Direct RF down converter
- High speed digital acquisition
- Radar and electronic countermeasure

Features

- Dual channel ultra-high speed A/D converter
- Resolution 8 Bits
- Single+1.9V±0.1V Operation
- Inter leave Mode for 2x Sample Rate
- Multiple ADC Synchronization Capability
- Duty Cycle Corrected Sample Clock
- Max Conversion Rate 1.5GSPS(min)
- DNL：±0.4LSB
- Serial Interface for Extended Control
- 4-bit address, 16 bit data
- Input full scale range digital adjustment

Description

CBM08AD1500 is made by CMOS process A semiconductor integrated circuit. This product combines folding and interpolation The circuit contains sample/hold amplifier and folding Amplifier, bandgap voltage reference, clock circuit and LVDS output Etc.

The circuit is packaged in a 128 lead four sided flat shell(TQFP128), overall dimension is 22mm × 22mm × 2mm, in accordance with GJB597A-1996.

The product features high sampling rate, low power consumption, small linear error Automatic gain and offset correction and 3-wire interface control.Gain, offset and connection of internal circuit can be realized through 3-wire interface The clock matching between channels is used for correction, and the analog input is differential input,Either AC coupling or DC coupling; Clock input circuit internal With DC offset, AC coupling input is required.

This product is compatible with foreign National Semiconductor companies The ADC08D1500 pins of the company's products are arranged in the same way, with the same function and performance It can directly replace ADC08D1500.

Functional block diagram

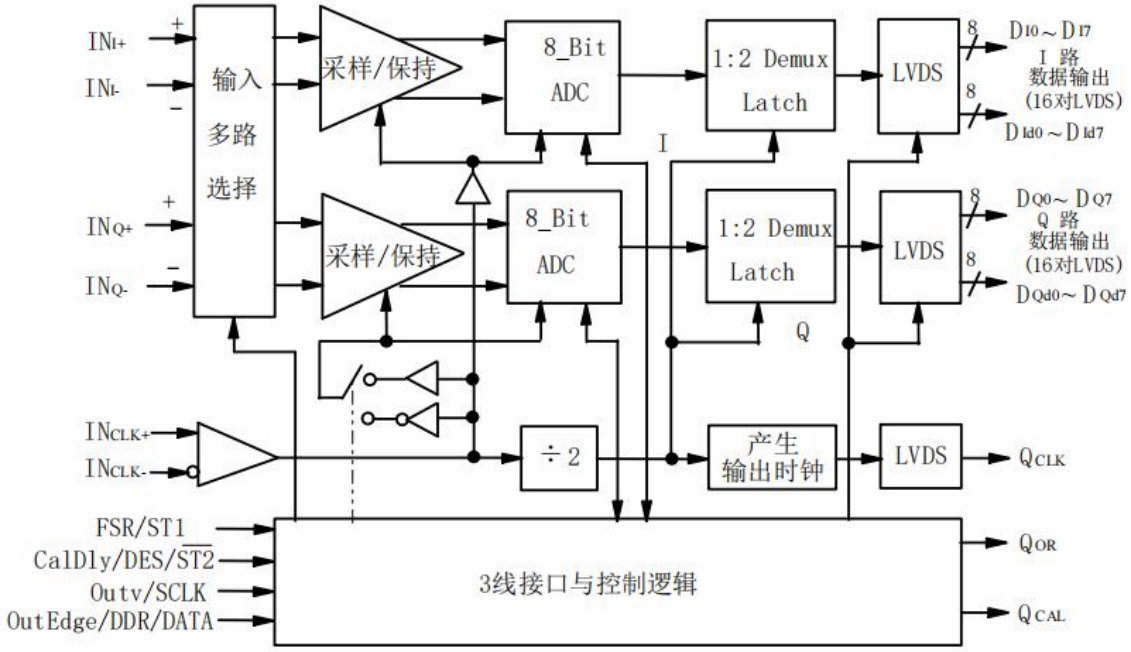


Figure 1. Functional block diagram

Timing diagram

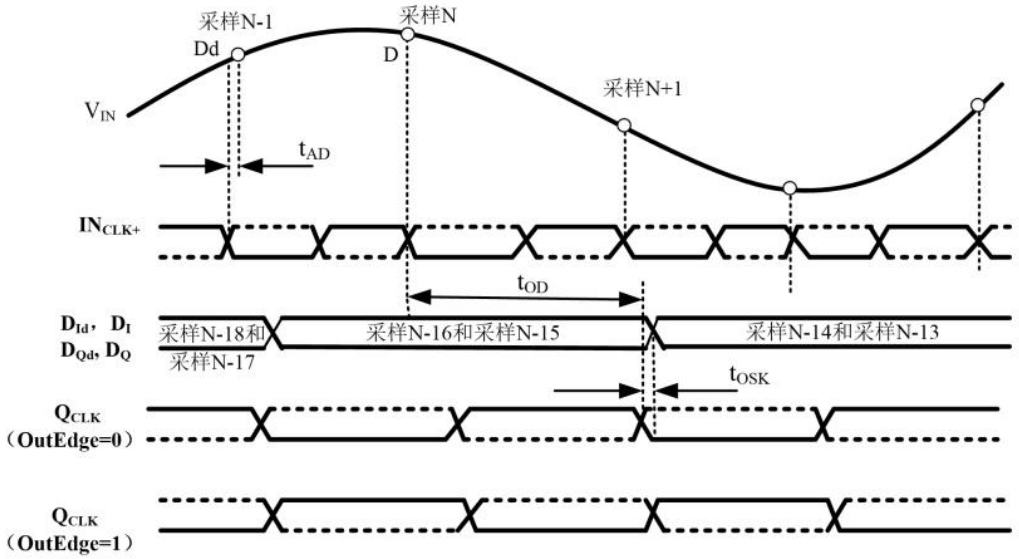


Figure 2. CBM08AD1500 single data rate (SDR) timing (OutEdge is high or low)

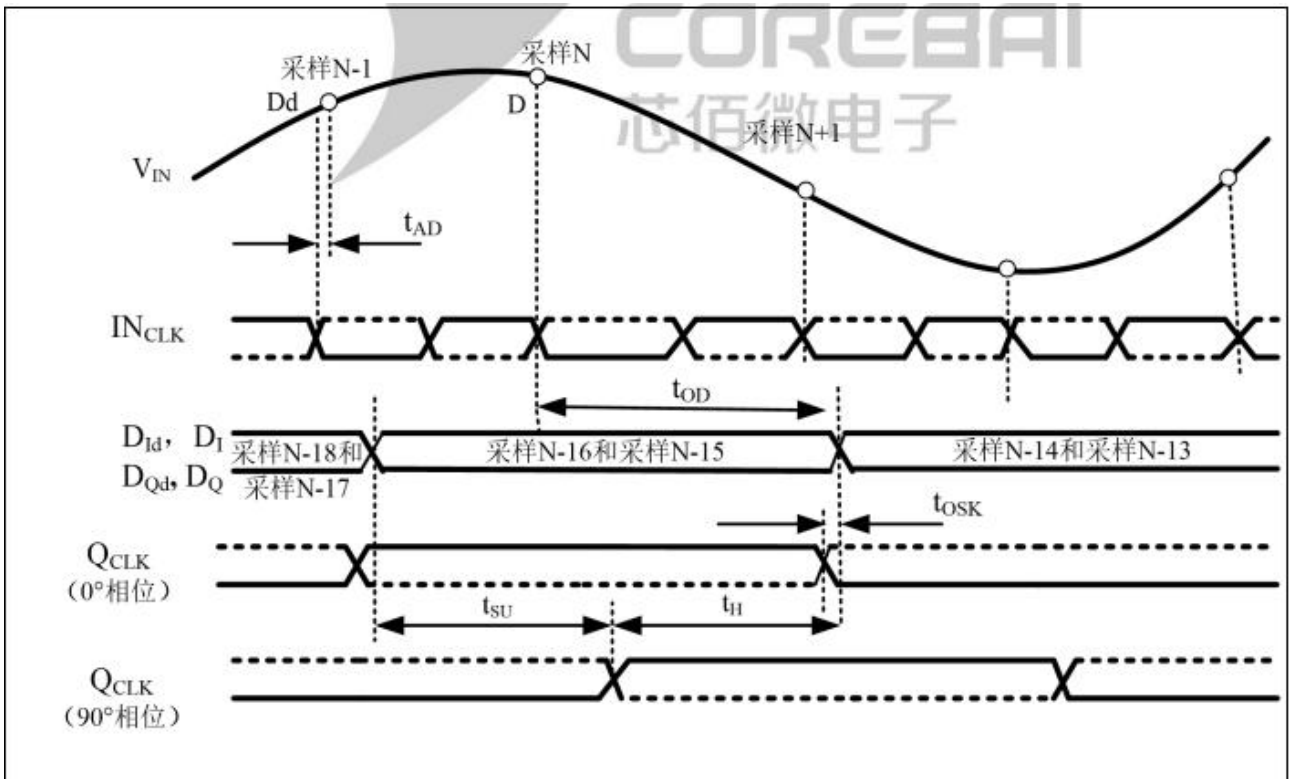


Figure 3.CBM08AD1500 Double Data Rate (DDR) timing (OutEdge hanging or VCC/2)

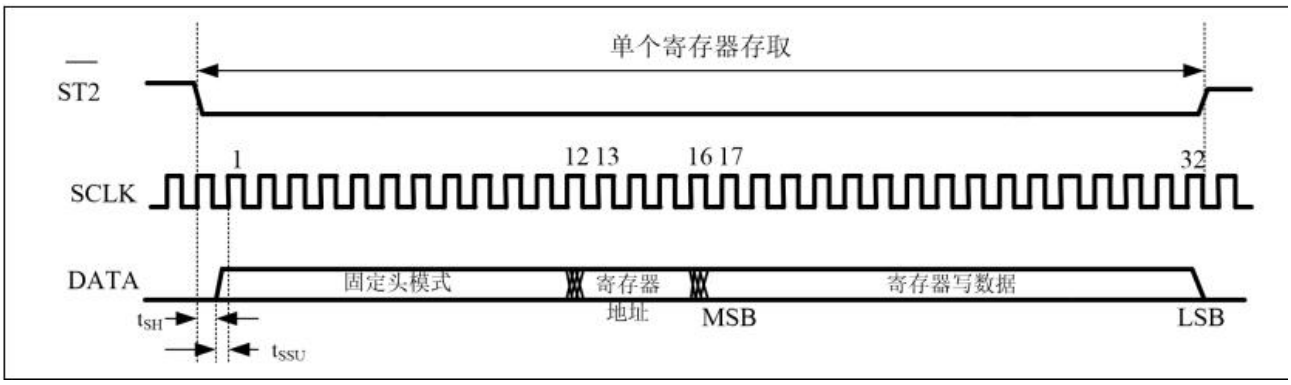


Figure 4.Serial interface timing

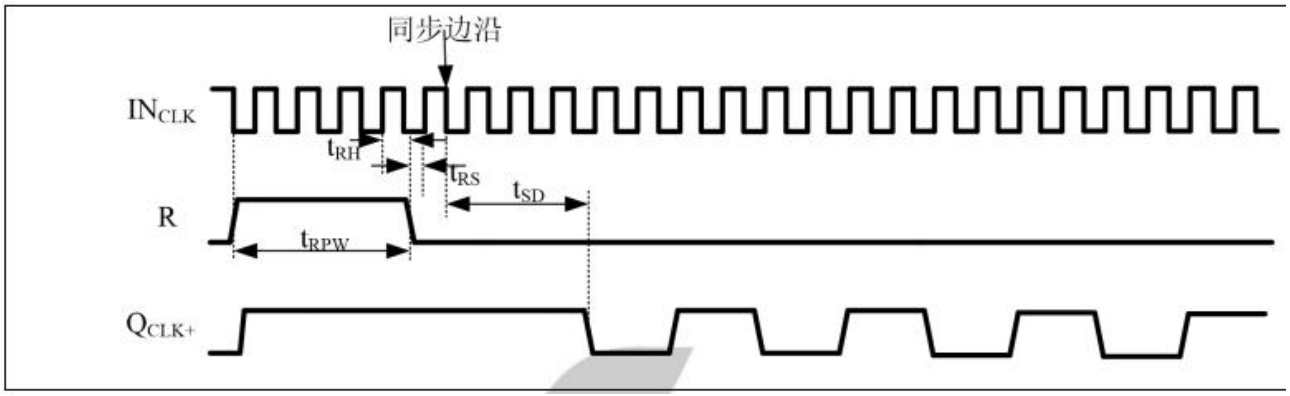


Figure 5.Clock reset timing in DDR mode when OutEdge is suspended or VCC/2

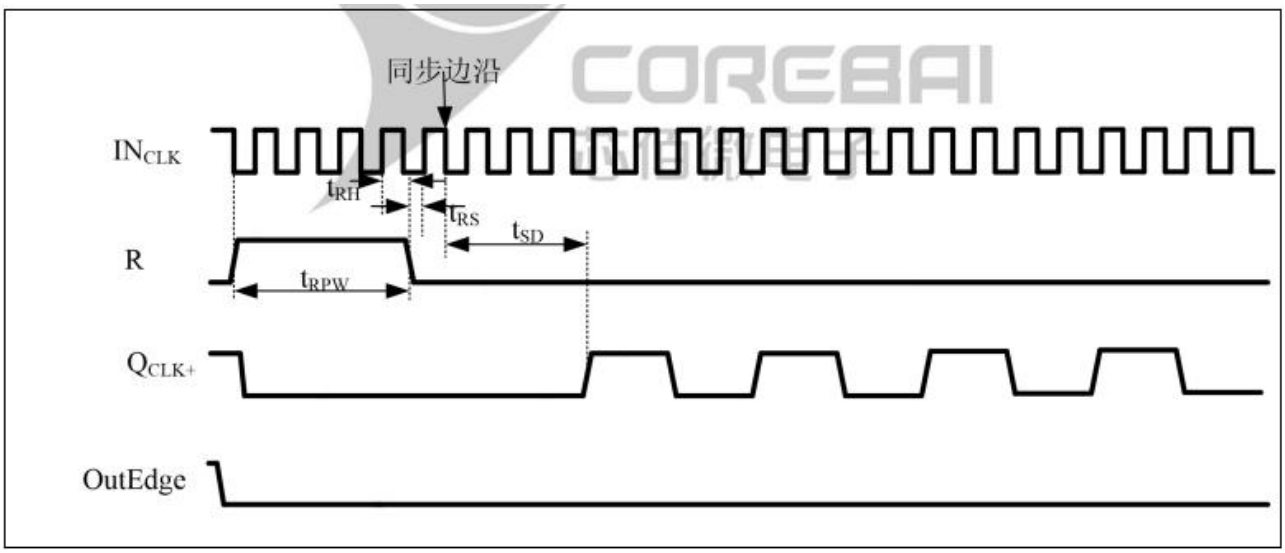


Figure 6.When OutEdge is low, the clock reset timing of SDR mode

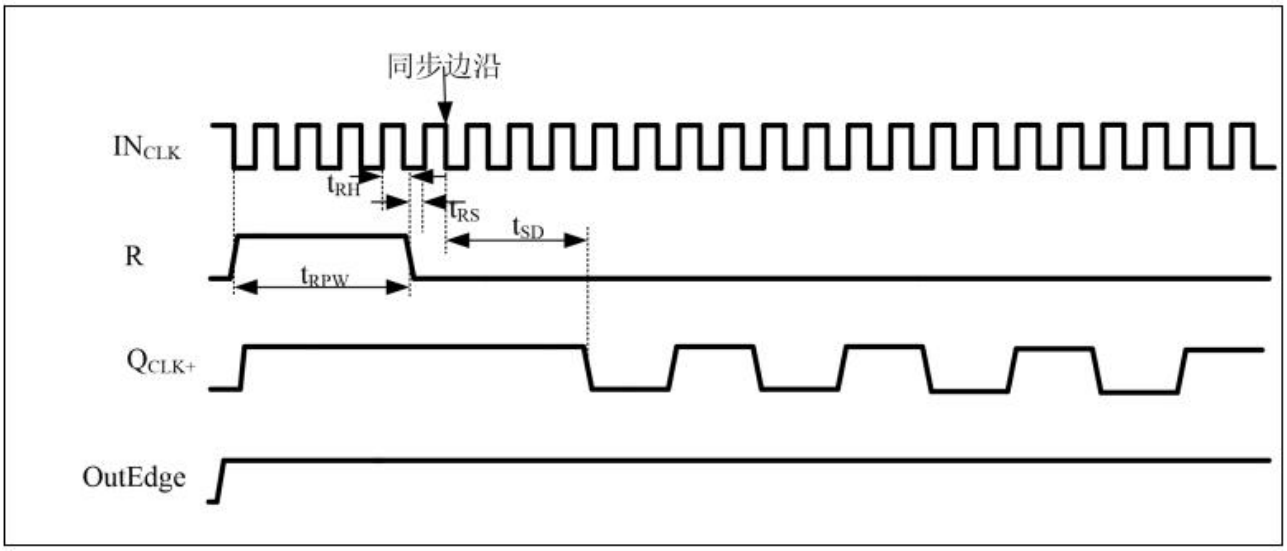


Figure 7.When OutEdge is high, the clock in SDR mode resets the timing

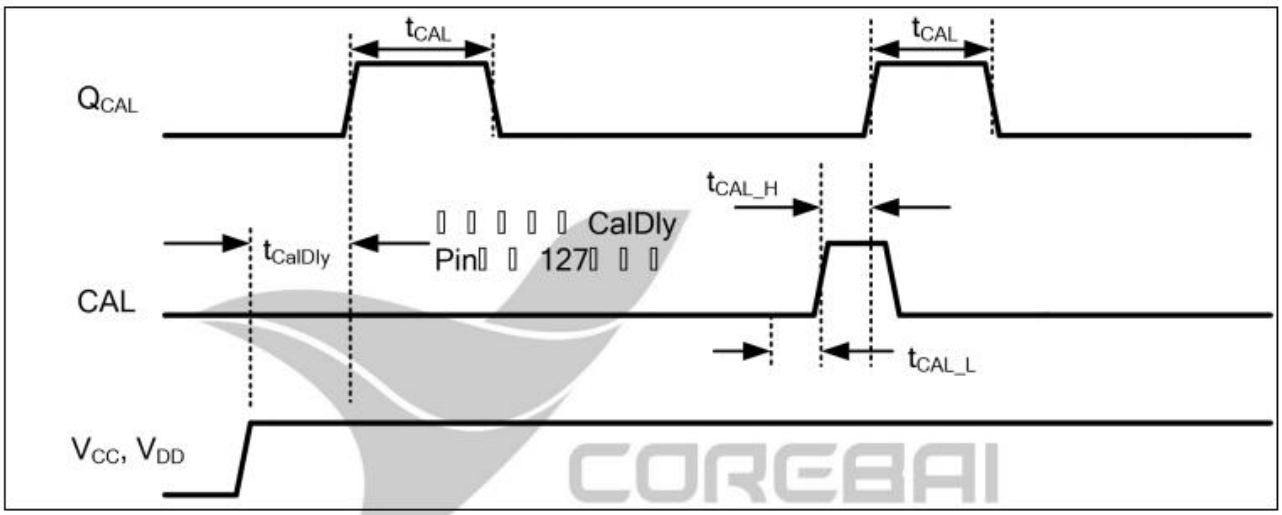


Figure 8.Self correction and instruction correction timing

Outcode

Equivalent decimal	V_{IN+} - V_{IN-}	Voltage level	Binary code	Overflow Bit
255	>460mV	>Positive Fullness Range + 1/2LSB	11111111	1
255	460mV	Positive Fullness Range + 1/2LSB	11111111	0
254	458mV	Positive Fullness Range - 1/2LSB	11111110	0
. .	. .		. .	
128	1.8mV	Bipolar 0 + 1/2LSB	10000000	0
127	-1.8mV	Bipolar 0 - 1/2LSB	01111111	0
. .	. .		. .	
1	-458mV	Negative Fullness Range + 1/2LSB	00000001	0
0	-460mV	Negative Fullness Range - 1/2LSB	00000000	0
0	< -460mV	< Negative Fullness Range + 1/2LSB	00000000	1

Table 1. Output Code (Standard mode, FSR high)

Recommended operation conditions

- Power supply voltage (V_{CC}, V_{DD}): 1.8V-2.0V
- Analog input common mode voltage: 1.26V +50mV
- Differential analog input range: 570-1100 mVpp
- Serial interface clock input frequency: 100MHz
- Clock frequency range: 200 MHz ~ 1500MHz
- Clock input duty cycle: 20%-80% (Typical 50%)
- Differential clock input amplitude: 0.5-2.0 V_{PP} (Typical 0.6 V_{PP})
- Operating temperature: -45 ~85 C

Absolute maximum rating

- Power supply voltage (V_{CC}, V_{DD}): 2.2V
- V_{DD}-V_{CC}: 0V ~ 100mV
- Input current of any pin: ± 25mA
- ESD protection: human model: 2000V, machine model: 250V
- Welding resistance temperature of lead wire TH (10s): 300 ℃
- Storage temperature T_S: - 65 ℃ ~ 150 ℃
- Junction temperature T_J: 175 ℃

Electrical characteristics

Unless otherwise specified, the electrical characteristics shall comply with Table 2. The electrical test method shall be in accordance with SJ 20961-2006. Analog input AC coupling, differential 920mVpp; Clock AC coupling input, duty cycle 50%; External resistance Rext=3300 Ω± 0.1%. Typical values in Table 3 are only reference data at 25 ℃.

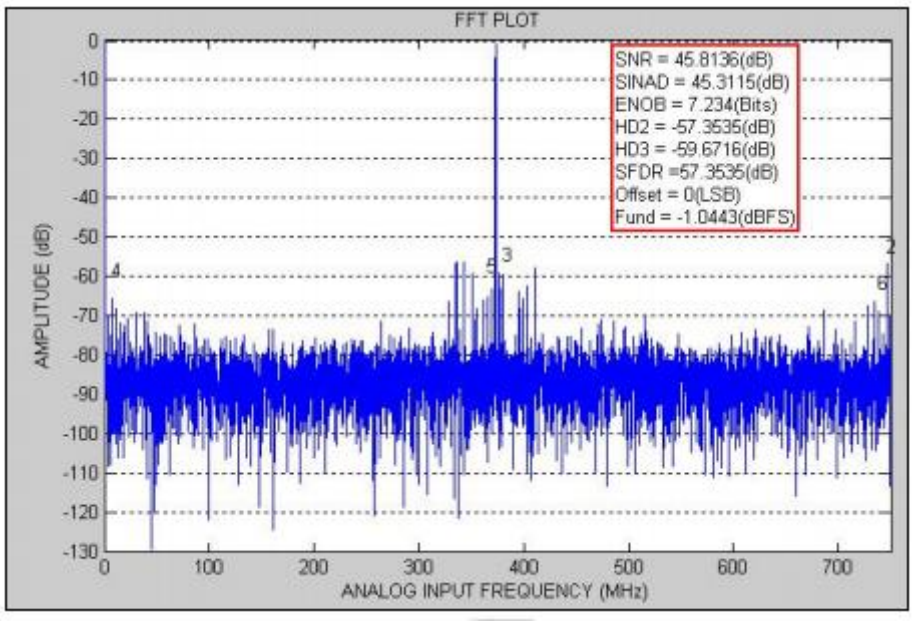
Parameter name	Symbol	Conditions (unless otherwise specified, V_{CC}=V_{DD}=1.9V, GND_A=GND_D=0V)	Electrical characteristics			CBM08AD1500	Unit
			Min	Typ	Max		
Resolution	RES			8		8	bits
Analog supply current	I_{CC}	PD = PDQ = 0V	--	900	930	≤870	mA
Digital supply current	I_{DD}	PD = PDQ = 0V	--	220	250	≤290	mA
Power	PD	PD = PDQ = 0V	--	2.0	2.2	≤2.2	W

consumption							
Integral Non-Linearity	E_L	DC Coupled, 1MHz Sine Wave Overranged	-1.2	±0.6	1.2	±0.9	LSB
Differential Non-Linearity	E_{DL}		-1.0	±0.4	1.0	±0.6	LSB
Offset Error	E_O		-2.5	-0.45	-2.5	-1.5~1	LSB
Positive Full-Scale Error	E_{FS+}		-40	±10	40	±25	mV
Negative Full-Scale Error	E_{FS-}		-40	±10	40	±25	mV
Bandgap Reference Output Voltage	V_{REF}	I_{REF} =±100μA	1.20	1.27	1.33	1.20~1.33	V
Analog differential input voltage	$V_{ID1(PP)}$	FSR pin 14 is low	570	700	900	570~730	mVp-p
		FSR pin 14 is high	790	920	1100	790~950	mVp-p
Analog differential input resistance	RI		94	100	106	94~106	Ω
Clock input differential voltage	$V_{ID2(PP)}$		0.5	0.6	2	0.4~2	V
Logic Low Input Voltage	V_{IL}	Outv，R，PD, PDQ	--		0.3	≤0.3	V
Logic High Input Voltage	V_{IH}		1.6		--	≥1.6	V
Digital output high level	V_{OH}	Q_{Cal} (126 pin)	1.5	1.65	--	≥1.5	V
Digital output low level	V_{OL}		--	0.15	0.3	≤0.3	V

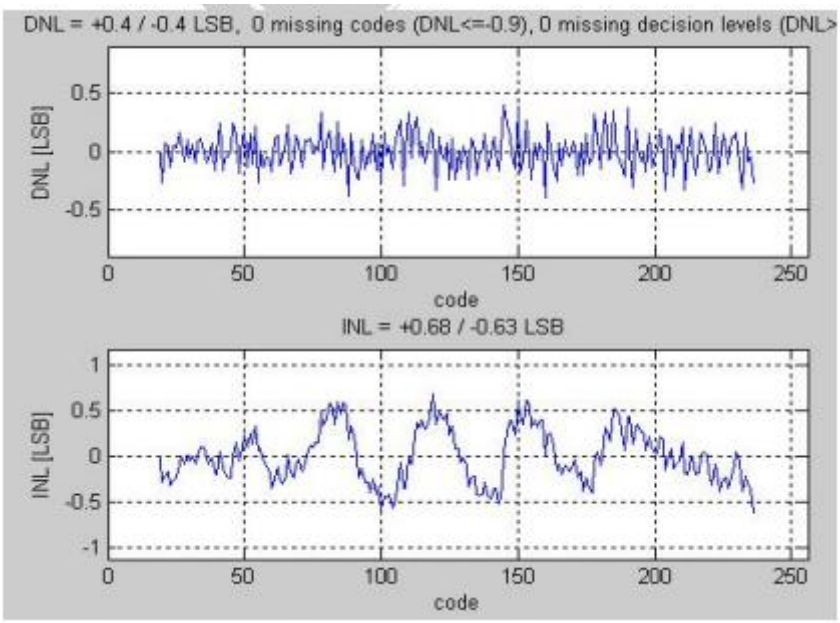
LVDS differential output voltage	$V_{OD\ (PP)}$	OutV= V_{CC}, V_{REF} no connect	400	700	1000	400~920	mV
		OutV= GND, V_{REF} no connect	280	500	800	280~720	mV
Out of Range Output Code	OROC	$(V_{IN+}-V_{IN-}) > +$Full Scale	255	--	--	≥255	--
		$(V_{IN+}-V_{IN-}) <$ -Full Scale	--	--	0	≤0	--
Gain Flatness	ΔA	dc ~ 500MHz	-1	±0.5	1	±1	dBFS
Signal-to-Noise Ratio	SNR	f_{CLK}=1.5GHz, f_{IN}=373MHz	42	45.0	--	≥44.5	dB
Effective Number of Bits	ENOB		6.6	7.2	--	≥7.0	Bits
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{CLK}=1.5GHz, f_{IN}=373MHz	41.5	44.5	--	≥43.9	dB
Spurious-Free dynamic Range	SFDR		45	54	--	≥48.5	dB
Total Harmonic Distortion	THD	f_{CLK}=1.5GHz，f_{IN}=373MHz	--	--	-45	-53.5（typ）	dB
Maximum conversion rate	S_{Rmax}	f_{IN} = 373MHz	1.5	--	--	≥1.5	GSPS
Output clock duty cycle	Q_{DC}		45	50	55	45~55	%

Clock setting pulse width	t_{RPW}	See Figure. 5~7 Timing	4	--	--	≥4	Clock cycle
Correction control input Low level time	t_{CAL_L}	See Figure. 8 Timing	80	--	--	≥80	Clock cycle
Correction control input High level time	t_{CAL_H}	See Figure. 8 Timing	80	--	--	≥80	Clock cycle

Characteristic curve



f_{clk}=1.5GSPS，f_{IN}=373MHz



fclk=1.5GSPS，fIN=373MHz

Application Description

1. Function Description

1) . General

The CBM08AD1500 adopts a folding and interpolation structure with correction, which can reach the effective bit of 7.1 bits. The application of folding operational amplifier greatly reduces the number of comparators and power consumption. The interpolation structure reduces the number of pre amplifiers, reduces the load capacitance of the input signal, and further reduces the power consumption. In addition, device integration correction reduces the INL bow caused by folding structure. Through these technologies, a converter with ultra-high speed, high performance and low power consumption is realized.

The analog input signal within the input voltage range of the converter is digitized into 8-bit code value for output, and the conversion rate is 200MSPS ~ 1.5GSPS. Under typical circumstances, the differential input voltage is lower than the negative full scale value, which will make the output code value all 0; If the differential input voltage is higher than the positive full scale value, the output code value will be all 1. In case of any of the above two conditions, the "I" or "Q" channel will overflow the output range. These single output code values are out of range, which means that the code values output from one channel or two channels are lower than the negative full scale value or higher than the positive full scale value. Both channel converters have a 1:2 multi-channel signal separator that meets the requirements of two LVDS

output buses. The data on these output buses is output at the rate of half the sampling rate on each bus. At the same time, the user can select interlaced scanning to achieve the rate output of the sampling rate.

The output amplitude can be normal mode or low amplitude mode. Using low amplitude mode can reduce power consumption but will cause some or all data acquisition, especially in high sampling rate and boundary design systems.

a. Self correction

Power on and user command can start self calibration. Self correction is mainly used to adjust the 100 Ω analog input differential terminal resistance, minimize the full scale error, offset error, DNL and INL, and maximize SNR, THD, SINAD and ENOB. Similarly, the internal bias current is also set through the self correction process. Power on self-tuning and user command startup self-tuning can achieve these purposes. Self calibration is a device function an important component, whose purpose is to make the device achieve better performance. In addition to the power on startup, the self calibration shall be restarted whenever the control of FSR pin (pin 14) changes. To achieve better performance, we recommend that the self-tuning run for 20 seconds or more after power on and when the device operating temperature is significantly different from the temperature required by the system performance. For more details, refer to 2.4). b. ② command correction. When the device is in power saving mode (PD or PDQ is high), self calibration cannot be initialized or run. For more detailed information, refer to 1.1). g The relationship between power saving mode self-tuning and power saving mode.

In normal operating mode, self calibration will work when the device is powered on and an effective calibration command is input. The correction command keeps the CAL pin (30 pin) low by at least one t_{CAL_L} clock cycle, and then keep the CAL pin high for at least another t_{CAL_H} Clock cycle, where t_{CAL_L} and t_{CAL_H} is defined in the electrical characteristics of the converter, see Figure 8. The time occupied by the self calibration is t_{CAL} defined in the electrical characteristics of the converter. Keeping the CAL pin high after power on will prevent the self-tuning process from running until the CAL pin appears the previously mentioned t_{CAL_L} clock cycle is followed by t_{CAL_H} Clock cycle.

CalDly (pin 127) is used to select one of the two delay times from power on to the start of self-tuning. The self-tuning delay time is set by CalDly pin, which is defined as t_{CalDly} in the electrical characteristics of the converter, as shown in Table 3. The length of these delay times is the time when the power supply voltage is powered on and stabilized to the self-tuning operation. If the PD (pin 26) is high after power on, the self-tuning delay calculator will not work until the PD pin is low again. Therefore, keeping the PD pin high after power on will further delay the start of

the self-tuning cycle after power on. The best setting of the CalDly pin depends on the power on setting time of the power supply voltage.

CalDly (pin 127)	Power on delay selection (t_{CalDly})
H	231 input clock cycles
L	225 input clock cycles
DES (double edge sampling mode)	225 input clock cycles

Table 3. Power on delay time control function table (PD is low level)

Precautions for self calibration:

● During the self-tuning cycle, the overflow (QOR) output may be a useful result of the correction algorithm. During calibration, all data output and overflow output data are invalid.

● During power on correction and instruction correction, the clock of internal ADC core and output clock QCLK stop working; At this time, the input terminal resistance is adjusted to Rext/33. The correction of input resistance in the correction period is a part of the correction period in order to reduce noise. Refer to 2.4). b. Self correction. This external resistance is between pin 32 and ground, Rext must be exactly 3.3kΩ ± 0.1%. With this value, the input terminal resistance is adjusted to 100 Ω. Because Rext is also used to set the appropriate bias current for the sample/hold op amp, pre amplifier, and comparator, other Rext values cannot be used.

● As long as the calibration is running, the CalRun output is high whether it is power on self-tuning or user command to start self-tuning.

b. Capture of output data

The data output at the falling edge of clock INCLK+(pin 18), that is, the data output at DI and DQ terminals after 13 input clock cycles and the data output at DId and DQd terminals after 14 input clock cycles are valid. Before the output data is obtained, there is another internal delay called t_{OD}, as shown in the sequence diagram. As long as there is an input clock signal, the CBM08AD1500 will perform data conversion. The full differential comparator design, innovative sample and hold amplifier design, and self-tuning technology have obtained a very flat SINAD/ENOB response below 1.5GHz. The output data signal of CBM08AD1500 is LVDS, and the output format is binary offset code.

c. Control mode

The multiple control pins provided realize multiple modes of user control. For example, it includes initialization of correction cycle, power saving mode and full scale range setting control. However, the CBM08AD1500 also provides an extended control mode. Through the extended control mode, a serial interface is used to access the control of many advanced characteristics based on registers. This extended control mode cannot be used automatically, and users want to use the normal control mode or extended control mode at all times. When the device is in the extended control mode, many characteristics of pin based control will be replaced by those of register based control, and those pin based controls will be invalid. These pins are Outv (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and CalDly/DES (pin 127), as shown in Table 4. For more detailed information about the extended control mode, please refer to 1.2) Common/Extended Control Mode.

Control input	**Functional pin**				
FSR/ST（pin14 ）	**Control mode**	**CalDly/DES/$\overline{ST2}$ （pin 127)**		**OutEdge/DDR/DATA (pin4)**	**Outv/SCLK （pin3)**
H or L (V_{CC} or GND)	Normal mode	Power on correction delay selection: Delay 2^{31}clock cycles at H; Delay 2^{25}clock cycles at L; Double edge sampling: suspended or $0.5V_{CC}$		Single data rate mode (SDR): H or L double data rate mode (DDR): suspended or $0.5V_{CC}$	Control LVDS output amplitude: Output normal amplitude at H; Output amplitude decreases at L
Suspended or $V_{CC}/2$	Extended mode	Clock and data of strobe extended mode serial interface	H	Serial data input blocked	Serial data input blocked
			L	Serial data input	Serial clock input

Table 4. Control Mode

d. Analog input

The CBM08AD1500 must be driven by a differential input signal, and single ended signal operation is not recommended. When AC coupling input, V_{CMO} (7-pin) is grounded; When DC coupling is input, the V_{CMO} pin is suspended, but the input common mode voltage must be equal to the output voltage of the V_{CMO}. Pin 14 (FSR) provides two full scale range settings. In the normal mode, the FSR setting controls the input full scale range, which is defined by the parameter analog input range in the electrical characteristics of the converter. The full scale range setting is valid for both ADC. In the extended control mode, the input full scale range is

adjusted by the data input of the serial interface, which is described in 1.4) and 2.2). See Table 5 for analog input full scale range control

FSR	Analog differential input full scale range
H	790～1100mVpp，920 mVpp（typ）
L	570～900 mVpp，700 mVpp（typ）
Suspended or $V_{CC}/2$	9-bit binary code input control of serial interface, 560-840 mVpp, default 700 mVpp

e. Clock input/output

The CBM08AD1500 must be driven by a differential clock signal through AC coupling connection. 2.3) describes the use of the clock input pin. A differential LVDS output clock is used to latch ADC output data for subsequent devices to receive data. The CBM08AD1500 provides two output clock options: one is to select whether the output data is converted at the upper edge of the output clock QCLK or at the lower edge of the output clock; the other is to select whether the output is single data rate (SDR) or dual data rate (DDR), as shown in Table 6, and the timing is shown in Figures 2 and 3.

OutEdge/DDR (pin4)	Mode	Output clock
H	SDR	The frequency is 1/2 of the input frequency, and the output data is converted on the upper edge of the clock
L		The frequency is 1/2 of the input frequency, and the output data is converted at the lower edge of the clock
Suspended or $V_{CC}/2$	DDR	The frequency is 1/4 of the input frequency, and the output data is converted on the upper and lower edges of the clock

Table 6. Output Clock Selection (FSR is H or L)

There is a duty cycle regulator inside the clock input of CBM08AD1500 to improve the performance of the internal clock. You can select whether the duty cycle regulator works through the extended mode (address code 0001). The default setting is working. The duty cycle regulator allows the clock of ADC to be a signal source with a duty cycle of 20-80% (worst case).

① . Double edge sampling (DES function)

DES mode allows one input (I or Q channel) of CBM08AD1500 to be sampled by two ADCs. One ADC samples the input signal at the positive edge of the input clock, and the other ADC samples the input at the negative edge of the input clock. Therefore, the signal input is sampled twice in each clock cycle, so a complete sampling rate is twice the input clock frequency, or the sampling rate for the 1.5GHz input clock is 3GSPS。

In this mode, the interleaved output data is converted to 1:4 by a multiplexer. Since the sampling rate is twice, under the 1.5GHz input clock, any of the four data outputs will be output at a rate of 750MHz, and all data will be output in parallel. The 4-way parallel data output by each clock follows the sampling sequence from the earliest to the last: D_{Qd}, D_{Id}, D_Q, D_I, that is, D_{Qd} at the earliest, followed by DId, and finally DI; This means that it is possible to provide different sampling rates. Double edge sampling In the general control mode, only the "I" analog input (INI) is available, and the "Q" analog input (I_{NQ}) is not used. In the extended control mode, the user can select any one ("I" or "Q") as the analog input to be sampled, and the address code is 1110. See Table 7 for control functions.

The CBM08AD1500 includes an automatic clock phase background correction feature, which can automatically and continuously adjust the clock phases of channel I and channel Q in DES mode. This feature eliminates the need to manually set the clock phase and provides the best bilateral edge sampling ENOB performance.

Special attention: The background correction feature in DES mode cannot replace the instruction correction to be run before entering DES mode, or the instruction correction required when the chip operating environment temperature changes greatly.

Data output (always corresponding to the falling edge of QCLK)	**General sampling mode**	**Double edge sampling mode (DES)**	
		Select I channel input	**Select Q channel input***
D_I	"I" input sampling corresponds to the falling edge of the first 13 IN_{CLK} cycles of the output	"I" input sampling corresponds to the falling edge of the first 13 INCLK cycles of the output	"Q" input sampling corresponds to the falling edge of the first 13 INCLK cycles of the output
D_{Id}	"I" input sampling corresponds to the falling edge of the first 14 IN_{CLK} cycles of the output	"I" input sampling corresponds to the falling edge of the first 14 INCLK cycles of the output	"Q" input sampling corresponds to the falling edge of the first 14 INCLK cycles of the output
D_Q	"Q" input sampling corresponds to the falling edge of the first 13 IN_{CLK}	"I" input sampling corresponds to the rising edge of the first 13.5	"Q" input sampling corresponds to the rising edge of the first 13.5

	cycles of the output	INCLK cycles of the output	INCLK cycles of the output
D_{Qd}	"Q" input sampling corresponds to the falling edge of the first 14 IN_{CLK} cycles of the output	"I" input sampling corresponds to the rising edge of the first 14.5 INCLK cycles of the output	"Q" input sampling corresponds to the rising edge of the first 14.5 INCLK cycles of the output

Table 7 Sampling Time of Input Channel Corresponding to Output Data

*DES normal mode, only channel I samples. In the extended mode of DES, I or Q channels can be sampled.

②. OutEdge pin settings

To make it easy to sample data in SDR mode, the output data can be converted on the positive or negative edge of the output data clock (Q_{CLK}). This can be selected via the OutEdge input (pin 4). When the OutEdge input is high, the output data is converted at the rising edge of Q_{CLK}; When the OutEdge input is low, the output data is converted at the falling edge of Q_{CLK}, as shown in Table 6. Refer to 2.4). c Output edge synchronization.

③ . Double data rate

Provides a choice of single data rate (SDR) or double data rate (DDR) output. If it is SDR, the output clock (Q_{CLK}) frequency is the same as the data rate of the two output buses. If it is DDR, the Q_{CLK} frequency is half of the data rate, and the data is sent to the output terminal at the two edges of the Q_{CLK}. The DDR clock is controlled by suspending pin 4 or V_CC/2. It is effective in the FSR (pin 14) common control mode, as shown in Table 4 and Table 6.

f. LVDS output

Data output, overflow output (D_{OR}) and clock output (Q_{CLK}) are LVDS. When the Outv input (pin 3) is high, the output current source will provide an output current of 3mA to a differential resistance load of 100 Ω; When the Outv input (pin 3) is low, the output current source will provide an output current of 2.2mA to a differential resistance load of 100 Ω, as shown in Table 8. In order to shorten LVDS line length and reduce system noise, Outv outputs.

If the input (pin 3) is low, satisfactory performance will be obtained while reducing power consumption. If the LVDS line is too long or the CBM08AD1500 system is too noisy, it is necessary to connect the Outv input to the high level. When V_{REF} (pin 31) is not connected or suspended, LVDS data output has a common mode voltage of 800mV. If higher common mode voltage is required, the common mode voltage can be increased to 1.2V by connecting V_{REF} pin to VCC, as shown in Table 9.

Special attention: connecting V_{REF} pin to V_{CC} will also increase the differential LVDS output voltage by 40mV.

Outv input (pin 3)	LVDS output amplitude
H	400～1000mVpp，700 mVpp(typ)
L	280～800mVpp，500 mVpp(typ)

Table 8. LVDS Output Amplitude Control

V_{REF} (pin 31)	LVDS output amplitude
H	1.2V(typ)
L	800mVp(typ)

Table 9. LVDS Output Common Mode Voltage (VOS)

g. Power Down

When PD (pin 26) is low, the CBM08AD1500 is in normal operation. When the PD pin is high, the device is in power saving mode. In the power saving mode, the data output pins (positive and negative) are tristate, and the device power consumption is minimized. Clock output ($Q_{\overline{CLK}}$ and Q_{CLK}) and overflow output ($D_{\overline{OR}}$ and D_{OR}) are not tri state, they are pulled to the ground internally. Therefore, when I and Q are both power saving modes Clock output and overflow output cannot be connected to a DC voltage. When the PDQ pin is high or suspended, the "Q" channel will be in the power saving mode, and the "I" channel will be in the normal working state, which is not controlled by the PDQ, as shown in Table 10. Back to the normal working mode, the channel will contain meaningless information. If PD is set to high during calibration operation, the device will not enter into power saving operation and will still work normally until the calibration timing is completed. However, if the device is powered on and the PD is high, the device will enter into power saving operation, and no correction will be made until the PD becomes low. If the device is in power saving mode and requires manual calibration, calibration will not start at all. That is to say, the manual correction input is completely blocked by the power saving state. However, if the PDQ is high, the "Q" channel is in the power saving mode, the "I" channel calibration will still run, and the "Q" channel cannot be calibrated. If the "Q" channel is used later, it is necessary to make a correction after the PDQ is low.

Power saving mode control		Operating mode	
PD	PDQ	I	Q
H	H or L	Power saving mode	Power saving mode
L	H or suspended	Normal operation	Power saving mode
	L	Normal operation	Normal operation

Table 10. Power saving mode control

2) . Common/extended control

The CBM08AD1500 can work in either of these two modes. Common standard control mode, users can set and control the working state of devices through several pins; "Extended control mode" is to realize additional configuration and control selection through a serial interface and the setting of 9 registers. Two control modes are selected through pin 14 (FSR/ST1: full scale range selection and extended control mode selection). The selection of control mode must be a fixed choice, and these two modes cannot be switched at will when the device is working. Table 11 shows that device characteristics are affected by control mode selection.

Characteristic	Normal control mode	Extended Control Mode
SDR or DDR mode clock	Pin 4 is suspended or VCC/2 selects DDR clock, SDR clock is selected for high or low	Select with nDE in the configuration register (1h; D10). When the device is in DDR mode, set the address 1h, and bit-8 must be 0.
DDR mode clock phase	No selection, only 0 ° phase	In the configuration register (1h; D11), select with DCP.
SDR mode, data conversion is on the rising or falling edge of QCLK	When pin 4 is high, SDR data is converted at the rising edge of QCLK+; When lead 4 is low, the falling edge switches	In the configuration register (1h; D8), select with OE
LVDS output amplitude	Pin 3 is high, normal differential data and Q_{CLK} output amplitude; When it is low, reduce the amplitude.	In the configuration register (1h; D9), select with OV
Power on correction delay	When pin 127 is low, select a short delay; For high, select a long delay.	Only a short delay

Full scale range	When pin 14 is high, the normal input full scale range; When it is low, reduce the range. Range selection is valid for both channels.	In the 1.4 register description, up to 512 steps are adjusted throughout the normal full scale range. Select the input full scale range adjustment register (3h; D7~D15)
Input maladjustment adjustment	Not adjustable	Adjust with input offset register (2h; D7~D15), up to 512 steps
Double edge sampling selection	Pin 127 suspended or $V_{CC}/2$	Control through DES enable register
Double edge sampling input channel selection	Only channel I input is available	Either I or Q channel input can be sampled by two ADC
DES sampling clock adjustment	The clock phase is automatically adjusted	Set D14 enable register (Dh) in DES to select automatic clock phase control. The clock phase can also be manually adjusted through the coarse and fine registers (Eh and Fh).

Table 11. Device Characteristics and Modes

The default state of the extended control mode is set by power on reset, as shown in Table 12.

Characteristic	**Extended Control Mode Default State**
SDR or DDR mode clock	DDR mode clock
DDR mode clock phase	QCLK edge (0° phase) data change
LVDS output amplitude	Normal amplitude (700m Vpp)
Power on correction delay	Reduced latency
Analog Input Full Scale Range	Both channels are 700mVpp
Input maladjustment adjustment	None misadjusted adjust
Double edge sampling (DES)	Do not use this mode

Table 12. Extended control mode operation (pin14 suspension or $V_{CC}/2$)

3) . Serial interface

The 3-wire serial interface can only be activated when the device is operating in the extended control mode. The pins of these serial interfaces are serial clocks(SCLK), serial data (DATA) and serial interface selection (ST2). Eight write only registers acquire signals through the serial interface.

ST2: When accessing a register through the serial interface, this signal should be low. Relative to the establishment time and retention time of SCLK requirements must be met.

SCLK: Serial data input is obtained at the rising edge of this signal, and there is no minimum frequency requirement for SCLK.

DATA: Each register access requires an explicit 32-bit combination format for this input. This format consists of header mode, register mode

Address and register value, and the register value starts from MSB bit. The establishment time and retention time relative to SCLK must meet the requirements sequence diagram.

Each register access consists of 32 bits, as shown in the sequence diagram in Figure 4. Fixed head mode is 0000 0000 0001, the writing order is 0, and the 12 bits constitute the header mode. Next, write the address of 4-bit register, and the last 16 bit data is write to the register. The addresses of different registers are described in detail in Table 13.

When $\overline{ST2}$ is permanently kept at low level, the subsequent register access from the 33rd SCLK can be directly completed no more strobe between. Although this usage is not recommended, it is possible.

Important note: When correcting ADC, do not use the serial interface. If it is used, the performance of the device will be reduced, unless it is correct again correction of. Serial interface register operation during register access will also reduce the dynamic characteristics of ADC.

4-bit address					
Address writing order: A3 is locked after H0 (the last bit of fixed head mode, i.e. "1"), and A0 is locked last					
A3	A2	A1	A0	Hex	Register address
0	0	0	0	0h	retain
0	0	0	1	1h	Status Configuration
0	0	1	0	2h	I channel input imbalance adjustment
0	0	1	1	3h	I channel full scale voltage regulation
0	1	0	0	4h	retain
0	1	0	1	5h	retain
0	1	1	0	6h	retain
0	1	1	1	7h	retain
1	0	0	0	8h	retain
1	0	0	1	9h	retain
1	0	1	0	Ah	Q channel input offset adjustment
1	0	1	1	Bh	Q channel full scale voltage regulation
1	1	0	0	Ch	retain
1	1	0	1	Dh	DES enable
1	1	1	0	Eh	DES coarse adjustment

1	1	1	1	Fh	DES fine regulation

Table 13. Register Address

4) . Register Description

In the extended control mode, the 8 write only registers provide many control and configuration options. When the device is in the normal control mode, these registers have no impact on the device. The following description of each register describes the power on reset state (POR) of each control bit.

Register Configuration

Address: 1h (0001b), write only. Default value: (0xB2FF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	DCS	DCP	nDE	OV	OE	1	1	1	1	1	1	1	1

Bit 15 must be set to 1b;

Bit 14 must be set to 0b;

Bit 13 must be set to 1b;

Bit 12 DCS: duty cycle stabilizer. When this bit is set to 1b, a duty cycle stabilizer circuit is applied to the clock input. When this bit is set to 0b, the duty cycle stabilizer circuit is cancelled. POR status: 1b

Bit 11 DCP: DDR mode clock phase. This bit can only be affected in DDR mode. When this bit is 0b, the QCLK edge is consistent with the data edge (0 ° phase). When this bit is 1b, the QCLK edge is located in the middle of the data binary unit (90 ° phase), using half the speed of QCLK. Refer to Figure 3 Phase. POR Status: 0b

Bit 10 nDE: DDR or SDR mode selection. When this bit is set to 0b, the data bus clock follows the DDR mode (double data rate), so that each rising and falling edge of the QCLK clock outputs a data byte. When this bit is 1b, the data bus clock follows the SDR mode (single data rate), so that the rising edge or falling edge of the QCLK clock outputs a data byte, which is determined by the OutEdge bit. POR Status: 0b

Bit 9 OV: output voltage amplitude. This bit determines the LVDS output voltage amplitude. It also has the same function as the OutV pin used in normal control mode. When this bit is 1b, the output standard amplitude is 800mVpp. When this bit is 0b, the output decreases by 600mVpp. POR status: 1b

Bit 8 OE: SDR mode output clock edge selection. This bit selects the QCLK edge of data conversion in SDR mode. It also has the same function as the OutEdge pin in normal control mode. When this bit is 1, the data output changes at the rising edge of QCLK+; When this bit is 0, the data output changes at the falling edge of QCLK+. POR Status: 0b

Bits 7:0 must be set to 1b.

I channel maladjustment regulation

Address: 2h (0010b), write only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB			offset value				LSB	sym bol	1	1	1	1	1	1	1

Bits 15:8 imbalance value. The input offset of channel I ADC is linearly and monotonically adjusted here. 00h provides a common zero offset, and FFh provides a 45mV offset. Therefore, each code step has an offset of 0.176 mV. POR status: 0000 0000 b

Bits 7 sign bit. 0b gives a positive imbalance and 1b gives a negative imbalance. POR Status: 0b

Bit 6:0 must be set to 1b

I channel full scale voltage regulation

Address: 3h (0011b), write only. Default value: (0x807F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB			offset value				LSB		1	1	1	1	1	1	1

Bit 15:7 Full scale voltage regulation value. The input full scale voltage or gain of the I-channel ADC is linearly and monotonously adjusted with a 9-bit data value.The adjustment range is ± 20% of the normal 700mVpp differential value.

0000 0000 0 560 mVpp

1000 0000 0 700 mVpp Default

1111 1111 1 840 mVpp

For best performance, it is recommended that this value be limited to 0110 0000 0b to 1110 0000 0b. For example, restrictions the adjustment range is ± 15%, and a margin of ± 5% is reserved to allow the ADC to change its full scale. The time of gain adjustment cannot be the same as ADC recalibration. POR status: 1000 0000 0b (not adjusted)

Bits 6:0 must be set to 1b

Q channel maladjustment regulation

Address: Ah (1010b); Write only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB			offset value				LSB	sym bol	1	1	1	1	1	1	1

Bits 15:8 imbalance value. The input offset of Q-channel ADC is adjusted here linearly and monotonously. 00h provides a common zero offset, and FFh provides a 45mV offset. Therefore, each code step has an offset of 0.176 mV. POR status: 0000 0000 b

Bits 7 sign bit. 0b gives a positive imbalance and 1b gives a negative imbalance. POR Status: 0b

Bit 6:0 must be set to 1b

Q channel full scale voltage regulation

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB			offset value				LSB		1	1	1	1	1	1	1

Bit 15:7 Full scale voltage regulation value. The input full scale voltage or gain of the Q-channel ADC is linearly and monotonically adjusted with a 9-bit data value. The adjustment range is ± 20% of the normal 700m VP-P differential value.

0000 0000 0 560 mVpp

1000 0000 0 700 mVpp Default

1111 1111 1 840 mVpp

For best performance, it is recommended that this value range be limited to 0110 0000 0b to 1110 0000 0b. For example, limit the adjustment to ± 15%. A margin of ± 5% is reserved to allow the ADC to change its full scale. ADC recalibration cannot be performed simultaneously during gain adjustment. POR status: 1000 0000 0b (not adjusted)

Bits 6:0 must be set to 1b

DES Enable Configuration

Address: Dh (1101b); Write only. Default value: (0x3FFF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DEN	ACP	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit 15 DES enable. Set this bit to 1b to enter the bilateral edge sampling mode. In this mode, the device operates in the time alternating mode. The analog input is sampled and converted

by dual ADC to obtain a sampling rate twice the input clock frequency. When this bit is set to 0b, the device operates in the normal dual channel mode. POR Status: 0b

Bit 14 Automatic Clock Phase Control (ACP). Set this bit to 1b to enter automatic clock phase control. In this mode, DES coarse and fine manual control is invalid. A phase detection circuit continuously adjusts the I and Q sampling edges to the phase beyond 180 degrees. When this bit is 0b, the sampling clock delay between I and Q channels is set to manual adjustment mode, and DES coarse and fine adjustment registers are used. (Refer to 2.4) .e） 。 It is recommended to use ACP control to set DES instead of manual setting. POR Status: 0b

Bit 13:0 must be set to 1b

DES coarse adjustment

Address: Eh (1110b); Write only. Default value: (0x07FF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IS	ADS	CAM			1	1	1	1	1	1	1	1	1	1	1

Bit 15 analog input selection. When this bit is set to 0b, the analog input of channel I works through two ADCs. When this bit is set to 1b, the input of Q channel works through two ADCs. POR Status: 0b

Bit 14 delay adjustment direction selection. When this bit is set to 0b, the program delay is used for the sampling clock of channel I, while the sampling clock of channel Q remains fixed. When this bit is set to 1b, the program delay is used for the Q channel sampling clock, while the I channel sampling clock remains fixed. POR Status: 0b

Bits 13:11 Delay coarse adjustment. Each code value here delays the sampling clock of I channel or Q channel (defined by ADS bit) by nearly 20ps. Here a value of 000b generates a 0 adjustment. POR status: 000b

Bits 10:0 must be set to 1b

DES fine regulation

Address: Fh (1111b); Write only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
(MSB)			FAM			(LSB)			1	1	1	1	1	1	1

Bits 15:7 Fine adjustment of delay. Here, each code value delays the sampling clock of channel I and channel Q (determined by ADS bit roughly adjusted by DES) by nearly 0.1ps. Here 0000 0000 0b is zero adjustment. Note that the size of each code value that can be adjusted varies

with the device operating environment and the selection of coarse adjustment value. POR status: 0000 0000 0b

Bit 6:0 must be set to 1b

a. A Note on Extended Mode Misalignment Correction

Please pay attention to the following information when using I or Q channel offset adjustment register.For the offset values of+0000 0000 and - 0000 0000, the actual values are different. Only need to change the sign bit in this case, both will have 1/10 LSB digital output code value. Figure 9 below shows it more clearly.

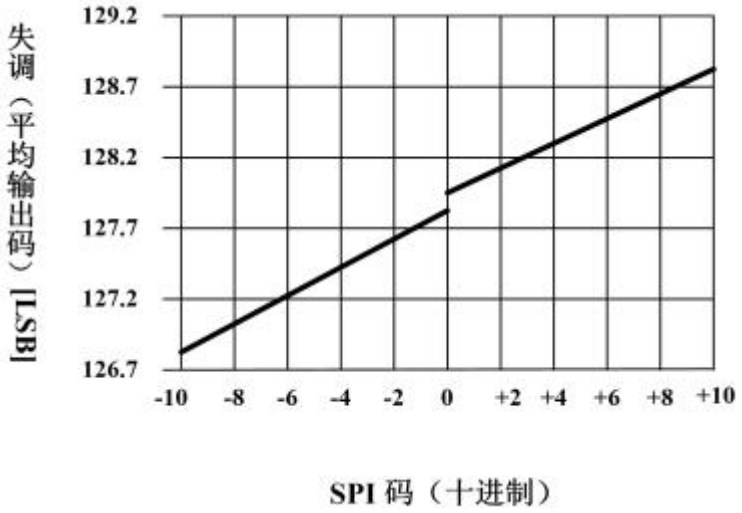


Figure 9. Expansion Mode Misalignment Performance

5）. Multiple ADC synchronization

The CBM08AD1500 has such a function that the user can input a set pulse R (pin 15) to precisely reset the relationship between the sampling clock input of the device and the QCLK output. This allows multiple ADCs to have their own QCLK (and data) output conversion in a system, and share the input clock INCLUD at the same time, which is used for all ADC samples. The set input R must meet the timing relationship shown in Figure 5, Figure 6 and Figure 7. The set pulse R must have a minimum width. With respect to the rising edge of the input clock INCLK, its falling edge must meet the requirements for establishing and holding time. These times are tRH, tRS and tRPW in the electrical characteristics of the converter. The set (R) signal is asynchronous with the input clock. If R is valid (logic high), the QCLK output is kept in a set state. The state maintained by QCLK during reset is determined by the operating mode (SDR/DDR) and OutvEdge configuration pin or configuration bit settings (refer to Figures 5, 6 and 7). Therefore, when the set bit (R) effectively realizes the clock reset, there may be a narrow pulse in the QCLK timing during the reset. When the R signal is not synchronized with the rising

edge of INCLK, the QCLK output at the falling edge of the next INCLK is synchronized with the output of other CBM08AD1500 in the system. After a fixed delay (relative to the input clock frequency), the QCLK output resumes, and the delay (tSD) from the instant clock input INCLK to the output clock QCLK. Under normal operation, the device always shows these delay characteristics. When the calibration process is in progress (when CalRun is high), the set (R) pin should not be set to high. Doing so will cause a digital pulse in the digital circuit, which will lead to errors and failures of correction.

2. Application information

1) . Reference voltage

The voltage reference of CBM08AD1500 is provided by a 1.254V bandgap reference with buffer. For the convenience of users, VREF can be obtained at pin 31. This output has a current output capacity of ± 100 μ A. If a larger current is needed, a buffer should be added. The internal bandgap reference voltage has a value corresponding to the common analog input value VID1, which is defined by the FSR pin and is in 1.1) D is described in the analog input.

This product does not provide the application of external reference voltage, but the full scale input voltage can be adjusted through a configuration register in the extended control mode, as described in 1.2) General/Extended Control. The differential input signal will be digitally converted into 8-digit code within the selected full scale input range. The part of the signal beyond the full scale range will not appear in the output. When the signal exceeds the full scale range, the overflow output DOR will be activated, refer to 2.2) B Overflow range indication. An additional feature of VREF pin is that it can be used to increase the output common mode voltage of LVDS. When VREF pin is used as output or not connected, the typical output common mode voltage (VOS) is 800mV. In order to increase the LVDS offset voltage to a typical value of 1200mV, the VREF pin can be directly connected to the power line.

2) . Analog input

The analog input is a differential signal that can be either AC coupled or DC coupled. In normal mode, the full scale input range is selected using the FSR pin. In the extended control mode, the full scale input range is selected by the full scale voltage regulation register through the serial interface. When adjusting the input full scale range in extended mode, for the best performance, refer to 1.4) Register description as a guide on the size limit of adjustment. Table 14 shows the relationship between input and output when SFR is high in normal mode, and the amplitude is reduced to 75% when SFR is low. In extended mode, this amplitude is determined by the full scale input range and offset setting of the control register. The analog input with buffer simplifies the case of driving these inputs. Generally, RC poles of sampled ADC inputs are

unnecessary. If an amplifier circuit is required before ADC, pay attention to selecting an amplifier with good enough noise and offset performance and sufficient gain at application frequency.

Note: an accurate DC common mode voltage must be applied to the analog input of ADC. When AC coupling is input, the common mode voltage V_{CMO} is provided by the device, and the analog signal is AC coupled to the input of ADC.

When the input is connected by AC coupling, the VCMO output must be grounded, as shown in Figure 10. The VCMO voltage inside the device is connected to the analog input through an on-chip 50K Ω resistor.

V_{IN+}	V_{IN-}	Out code
V_{CMO}-230mV	V_{CMO}+230mV	00000000
V_{CMO}-115mV	V_{CMO}+115mV	01000000
V_{CMO}	V_{CMO}	01111111 10000000
V_{CMO}+115mV	V_{CMO}-115mV	11000000
V_{CMO}+230mV	V_{CMO}-230mV	11111111

Table 14. Relationship between differential input and output (FSR is high, non extended mode)

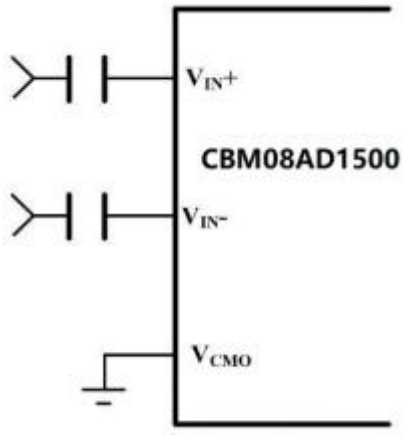


Figure.10 Differential input drive

Important note: When the analog input is AC coupling connection, the unused analog input channel (such as in DES mode) should be suspended, and the unused analog input should not be connected to the ground. When the analog input is DC coupled, the common mode voltage

must be provided at the differential input. This common mode voltage should track the VCMO output pin. Note that the VCMO output voltage will change with temperature, and the common mode voltage output of the drive circuit should track this change.

Important note: When analog input is DC coupled, unused analog input channels (such as in DES mode) should be connected to VCMO voltage, and unused analog inputs should not be connected to ground. When the input common mode voltage deviates from the VCMO, the full scale distortion performance drops very quickly, which is the direct result of using a very low power supply voltage to reduce power consumption. Therefore, the input common mode voltage should be kept within VCMO ± 50mV. The performance of the DC coupling connection mode of the CBM08AD1500 is as good as that of the AC coupling connection mode, but the input common mode voltage provided should be kept within VCMO ± 50mV under both modes.

a. Single ended input signal processing:: Because there is no circuit for single ended signal processing in the CBM08AD1500, it does not provide single ended input signal processing. The best way to process single ended signal is to convert the signal into differential signal before input to ADC. The easiest way to convert single ended signal into differential signal is to use an appropriate transformer with unbalanced connection, as shown in Figure 11.

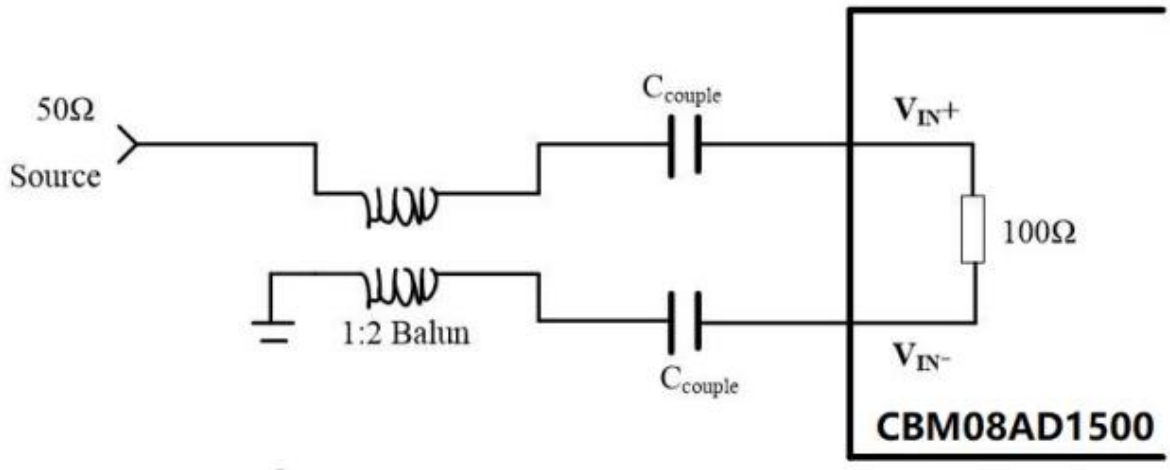


Figure 11. Single end to differential signal conversion

1. AC coupling input

The easiest way to convert a single ended AC input to a differential AC input is to use an appropriately unbalanced connected transformer, as shown in Figure 11. Figure 11 is a diagram of transforming single ended signal into differential signal by transformer. The characteristics of the transformer depend on the selection of the transformer type and the layout of the entire

board. It is suggested that the system designer communicate with the transformer manufacturer, who can help to select the best special transformer for single ended differential conversion.

When selecting a transformer, it is very important to understand the input structure of ADC. The system designer should pay attention to these special transformer parameters. The impedance from their analog input source to the 100 Ω differential input terminal resistor inside the CBM08AD1500 device should match. The range of this terminal resistance is described in the electrical characteristics table as RIN. As a result of ADC structure, the balance of phase and amplitude also becomes important. When a transformer is selected, the phase imbalance shall not exceed ± 2.5 °, and the amplitude imbalance within the desired input frequency range shall not exceed 1dB. Finally, VSWR (voltage standing wave ratio), bandwidth and insertion loss of the transformer should be considered. When connected to the ADC input, the VSWR helps determine the entire transmission line terminal capacitance of the transformer. Insertion loss shall be considered so that the signal output from the transformer is within the ADC input range VID1 required in the electrical characteristics.

2. DC coupling input

When DC coupling is required to CBM08AD1500 analog input, the single end to differential conversion is shown in Figure 12. In this application, the role of amplifier A1 is to achieve single end to differential conversion, transmit low offset and low noise signals at the same time, achieve output balance, and provide signals for CBM 08AD1500 to work. Connect V_{CMO} pin of CBM08AD1500 to V_{CM_REF} pin, through the proper buffer, will ensure that the common mode input voltage of the CBM08AD1500 is required for the optimal performance of the CBM08AD1500, as shown in Figure 12. Amplifier A2 in Figure 12 acts as a buffer with low voltage operation and reasonable offset voltage. Ensure that the current output from the CBM08AD1500 V_{CMO} pin does not exceed 100 μ A.

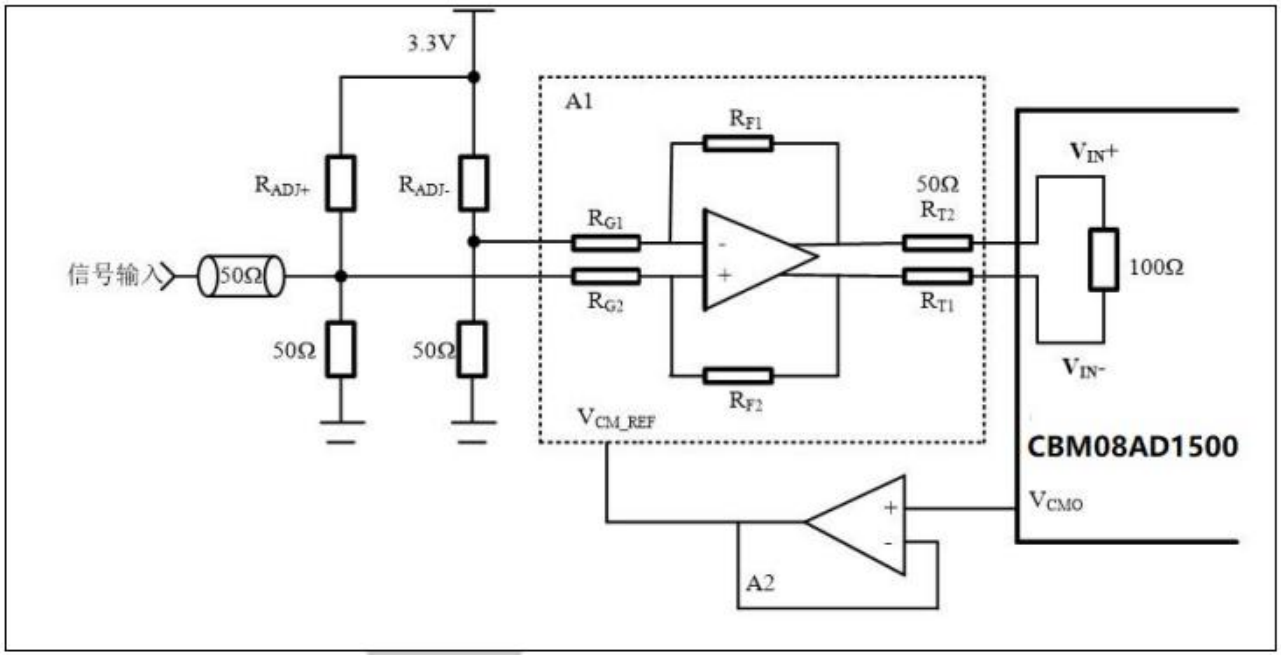


Figure 12. Example of analog input with V_{CMO}

R_{ADJ-} and R_{ADJ+}in Figure 12 are used to adjust differential misalignment, which can be measured from the ADC input V_{IN+}/V_{IN-}. With respect to the unadjusted positive offset of a V_{IN-} that exceeds | 15mV |, it should be reduced by the resistance at the R_{ADJ-} position. Similarly, an unadjusted negative offset with V_{IN-} exceeding | 15mV | should be reduced by the resistance at RADJ+. It is necessary to reduce the V_{IN+}/V_{IN-} differential offset to the value of | 15mV | with the unadjusted differential offset. The given R_{ADJ-} and R_{ADJ+}values are different, as shown in Table 15.

Unadjusted maladjustment reading	**Resistance value**
0mV to 10mV	No resistance required
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ

71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

Table 15. DC coupling maladjustment regulation

b. Overflow range (D_{OR}) indication

When a part of the conversion result is truncated, the overflow output is activated, and the result $D_{\overline{OR}}$ is high and D_{OR} is low. As long as the correct data on one or two buses is outside the range of 00h to FFh, this output will be activated.

C. Full scale input range

For all A/D converters, the input range is determined by the ADC reference voltage value. The reference voltage of the CBM08AD1500 is driven by an internal bandgap reference, and its effective reference voltage value is controlled by the FSR pin. Therefore, when the FSR pin is high, the differential full scale range of the analog input is normal; When the FSR pin is low, the reduced amplitude is defined in the electrical characteristics table. The best SNR is obtained when FSR is high, but better distortion and SFDR are obtained when FSR is low.

3) Clock input

The CBM08AD1500 has differential LVDS clock inputs $IN_{CLK+}$and IN_{CLK-}, and the clock input must be driven by differential signal AC coupling. The CBM08AD1500 uses a differential 1.5GHz clock to test and ensure its performance. This frequency is used in the electrical characteristic meter to represent typical functions. The clock input is internally provided with DC bias, and the input clock signal must be capacitively coupled to the clock pin, as shown in Figure 13.

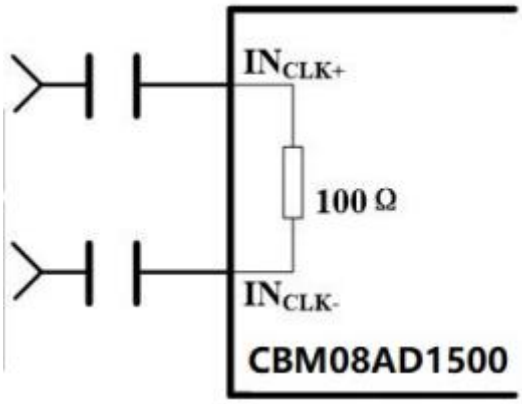


Figure 13. Differential (LVDS) input clock connection

If the maximum ambient temperature does not exceed the given range, there is no problem to work at the sampling rate defined by the conversion characteristics. If the working sampling rate exceeds the value given by the conversion characteristics at a given ambient temperature, the dynamic performance of the device may be reduced. This is because high sampling rate will result in high power consumption and chip temperature. Proper heat treatment in terms of reliability is also important. See 2.6) B Description of heat treatment. The clock input differential pair should have a characteristic resistance of 100 Ω . When a transformer is used, a characteristic resistance (100 Ω) should be connected to the clock source terminal. The input clock line should be as short and straight as possible. The CBM08AD1500 clock input has an unmodified 100 Ω resistor. Insufficient input clock amplitude will lead to poor dynamic performance, and excessive input clock amplitude will cause changes in analog input offset voltage. To avoid these problems, it is important to keep the clock amplitude within the given range of electrical characteristics V_{ID2}. The high and low time of the input clock signal will affect the performance of any A/D converter. The CBM08AD1500 has a clock duty cycle correction circuit to ensure the performance in the entire temperature range. If the high and low time of the input clock remain within the duty cycle range given by the electrical characteristics, the ADC will meet the performance requirements.

High speed and high performance ADC such as CBM08AD1500 requires a very stable input clock signal with minimum phase noise or jitter. ADC jitter is determined by ADC accuracy (bits), maximum input frequency, and input signal amplitude relative to the input full scale range. The maximum jitter (sum of jitters of all signal sources) to prevent SNR reduction caused by jitter can be obtained by the following formula:

$$t_{J(MAX)} = \frac{V_{INFSR}}{V_{INPP}} \times \frac{1}{2^{N+1}\pi \times f_{IN}}$$

Here $t_{J\ (MAX)}$ is the sum of the second-order root mean square of all dithering sources, $V_{IN\ (PP)}$ is the peak to peak value of the analog input signal, V_{INFSR} is the full scale range of ADC, "N" is the ADC resolution, and fIN is the maximum analog input frequency of ADC. Note that the maximum jitter mentioned above is the sum of RSS (square root of the sum of squares) of all source jitters, including the ADC input clock, plus the system to input clock and input signal, plus the jitter of the ADC itself. Since the ADC jitter is not controlled by the designer, the best that the designer can do is to ensure that the input clock jitter and the analog circuit to analog signal jitter add up to the minimum. If the input clock amplitude is greater than the value given in the electrical characteristics table, the input offset voltage will increase. When two analog

input pins are connected at the same potential, the converter will generate an unexpected 127/128 output code.

4) . Control pin

The six control pins (excluding the use of serial interfaces) provide many possible working modes of the CBM08AD1500 and help with the use of devices. These control pins provide full scale input range setting, self-tuning, correction delay, output edge synchronization selection, LVDS output level selection, and a power saving operation mode.

a. Full scale input range setting

In the normal working mode, the full scale input range is selected by the FSR control pin (pin 14), which is defined in the electrical characteristics table. The full scale input range in extended control mode (SPI mode) is controlled by SPI programming.

b. Self correction

The CBM08AD1500 must run self-tuning to achieve the guaranteed performance. The calibration process is automatic operation when powered on, and can also run at any time through command calibration. Whether there is an input clock after power on or a clock after power on for a period of time, the correction process is the same. CalRun output indicates high when calibration is running. Note that the Q_{CLK} output is invalid in the calibration cycle, so it is not recommended as the system clock.

① Power on correction

The correction process is automatically completed after a power on delay. This delay time is determined by CalDly settings and will be described in the correction delay selection section below. When power on, if the CAL pin is at high level, the calibration process cannot be completed, but the CBM08AD1500 will still work, but the calibration process cannot be executed. At this time, the performance will also deteriorate, and it is not recommended. In this case, instruction correction can be used to achieve correction. See 2.4). b. ② Instruction Correction for detailed description.

If the input clock does not run after power on and the power on correction circuit is active, then the internal power on correction circuit is in an unknown logic state. The analog circuit will remain in the power saving state, and the typical power consumption will not exceed 200mW. The power consumption will be normal after the clock starts running.

② . Command correction

Command correction can be run at any time. In order to start command correction, keep the minimum tCAL_L after input clock cycle, let CAL pin keep a minimum t_{CAL_H} Input clock cycle. If the CAL pin is high during power on, it will prevent the operation of power on correction. At

this time, the command correction method should be used to make the correction run, that is, the CAL pin must be low and keep the minimum t_{CAL_L} After the clock cycle is input, keep the minimum t_{CAL_H} Input clock cycle, CAL pin is at this high level t_{CAL_H} The calibration operation starts after the clock cycle is input. To determine when the calibration run is complete, the CalRun signal should be monitored. When no correction is required, in order to ensure that random noise does not cause correction to start, the minimum t_{CAL_H} and t_{CAL_L} Input clock cycle timing is required. Like in 1.1) A. For the best performance, the self-tuning should run for 20 seconds or more after power on. According to the actual system performance requirements, the calibration should be restarted when the operating temperature changes too much. ENOB decreases slightly with the increase of junction temperature. Running a new self-tuning cycle can fundamentally eliminate this change. During a power on correction cycle, both ADC and input terminal resistance are corrected. When ENOB changes slightly with junction temperature, executing a command correction can make ADC performance consistent.

③ . Correction delay

The CalDly input (pin 127) is used to select one of the two delay times from the power on application to the start of correction, such as 1.1) A Self correction. The value of correction delay time is to power on and stabilize the power supply voltage before the correction starts. There is no delay or insufficient delay, so that the correction will start to work when the power supply voltage has not stabilized at the operating value, which will lead to the failure to achieve the best correction result. If PD leads after power on

If the pin is high, the correction delay counter will fail until the PD pin is low. Therefore, keeping the PD pin high during power on will cause a greater delay in the start of power on correction. The best setting of the CalDly pin depends on the power on setting time of the power supply voltage.

Note: Correction delay selection in extended control mode is not available, and the delay time is shortened.

c. Output edge synchronization

The Q_{CLK} signal can be used to help the latch converter output data to the external circuit, and the output data can be synchronized with any edge of these Q_{CLK} signals. That is to say, the output data conversion can be set to occur on the rising edge or falling edge of the Q_{CLK} signal, so both edges of the Q_{CLK} signal can be used to latch the output data to the receiving circuit. When OutEdge (pin 4) is high, the output data conversion changes synchronously with the rising edge of Q_{CLK+}(pin 82); When OutEdge (pin 4) is low, the output data conversion changes synchronously with the falling edge of Q_{CLK+}(pin 82). At the very high speed that the

CBM08AD1500 can withstand, the slight difference between Q_{CLK+} and data line length can cause correct and wrong data capture. OutEdge pin is used to capture data at Q_{CLK+} edge, which is most suitable for application circuit and layout.

Important note: In order to obtain correct data, when the OutEdge (pin 4) is high, it is better to capture data with the falling edge of Q_{CLK+}; When OutEdge (pin 4) is low, it is better to capture data with the rising edge of Q_{CLK+}.

d. LVDS output level control

The output level can be set to one of the two levels with Outv (pin 3). When Outv is high, the output drive capability is very strong; When Outv is low, the output drive power consumption is low, but a smaller output level means that the noise resistance is reduced. For short LVDS lines and low noise systems, low Outv input can achieve satisfactory performance. If the LVDS line is very long or the system using the CBM08AD1500 is noisy, it is necessary to connect the Outv to high.

e. Bilateral edge sampling

The double edge sampling (DES) feature enables one pair of two analog inputs to be sent to the two channel ADC, while the other pair of inputs is invalid. One channel's ADC samples the input signal at one edge of the input clock (duty cycle correction), and the other channel samples the input signal at the other edge of the input clock (duty cycle correction). The result is that a 1:4 multiplexer outputs data, and the sampling rate is twice the input clock frequency. In order to use this feature in the non extended control mode, pin 127 is suspended, and the signal input in channel I is sampled by two converters, then the correction delay will be only a short delay. In the extended control mode, each input can be used as bilateral edge sampling, refer to 1.1). e. ①.

Important:

1) For the extended control mode, when the automatic clock phase control feature is used in the bilateral edge sampling mode, it is very important to set the automatic phase control to invalid (set bit 14 of DES enable register Dh to 0) before the ADC is powered on. If this is not done, the chip may not be able to switch from the power saving state to the normal working state.

2) For non extended control mode, when the CBM08AD1500 is powered on and DES mode is necessary, ensure that pin 127 (CalDly/DES/ST2) is initially low during or after the power on sequence, and then this pin can be suspended or connected to $V_{CC}/2$ to enter DES mode, which will ensure that this part correctly enters DES mode.

3) If the input clock is interrupted or stopped for some reason, the automatic phase control should also be invalid. If there is a big jump in the input clock frequency, it is also an example of this situation.

4) In automatic DES mode, if ADC calibration is necessary, the device must return to normal mode before completing a calibration cycle. Once the calibration is completed, the device can return to the automatic DES mode and start working again.

f. Power Down feature

The power saving pins (PD and PDQ) allow the CBM08AD1500 two channels to be completely in the power saving mode (PD) or the Q channel to enter the power saving mode while the I channel still works normally. See Table 10. For a more detailed introduction of power saving characteristics, see 1.1) Section g. When the power saving pins (PD and PDQ) are high to their respective channels, the data (+/-) output pins are in a high impedance state. From the power saving mode to the normal mode, the channel will contain meaningless information, which must be cleared. When the calibration is running, even if the PD input is high, the device cannot enter the power saving mode until the calibration process is completed. However, if power is on and PD is high, the device will not enter the calibration process until the PD input is low. When the device is in the power-saving mode, even if manual correction is used, the correction will not run at all. That is to say, when the device is in the power-saving mode, manual correction does not work and is completely blocked.

5) . Data output

Inside the device, the output data of I or Q channel in the CBM08AD1500 is sent to two LVDS output buses. One of the two LVDS buses starts to obtain output data continuously at the odd falling edge of the input clock (IN_{CLK+}) pin, while the other one starts to obtain output data continuously at the even falling edge of the input clock (IN_{CLK+}). This means that the data rate of each LVDS bus is half of the input clock frequency. At the same time, the two buses must be multiplexed to obtain a complete 1.5GSPS conversion result. Since the minimum input clock frequency recommended by this device is 200MHz (normal mode, non DES mode), the effective output data rate is as low as 100MSPS. Here is an LVDS output clock pair (QCLK) that can be used to latch LVDS output data on all buses. The data is in Q_{CLK}

The output of rising edge or falling edge is determined by the state of OutEdge pin, see 2.4) Part C. The DDR (double data rate) clock can also be used. In this mode, a group of data is output at each edge of the Q_{CLK}. The frequency of the Q_{CLK} is 1/4 of the input clock frequency. See the timing chart for more details.

Outv pin is used to set LVDS differential output amplitude, see 2.4) Part d. The output format is offset binary code. Therefore, an IN+positive full scale input relative to IN - will generate an output code that is all 1, and an IN - full scale input relative to IN+will generate an output code that is all 0. When IN+is equal to IN -, the output code will change between 127 and 128.

6）**. Power consumption considerations**

If the A/D converter does not fully bypass the amplified transient current, the internal power circuit will be damaged. At the A/D converter power

A 33 μ F capacitor should be placed within 2.5cm of the source pin, while another 0.1 μ F capacitor should be placed as close as possible to each VCC pin, preferably within 0.5cm. Lead free chip capacitors are preferred because of the low lead inductance. VCC and VDD power supply pins should be isolated to prevent digital noise coupling to the analog part of the ADC. When they share a power supply, it is recommended to place a ferrite choke between these power lines. As an example of all high-speed converters, suppose that the CBM08AD1500 has very small power supply voltage noise suppression. In a system that consumes a lot of digital power, any power supply used for digital circuits cannot be used as the power supply of the CBM08AD1500. If there is no special power supply, ADC power supply should use the same power supply as other analog circuits.

a. Supply voltage

The working power supply voltage specified by CBM08AD1500 is 1.9V ± 0.1V. It is important to note that when the device operates at a slightly higher power supply voltage, these higher power supply voltages may reduce the working life. The voltage of any pin shall not exceed the supply voltage or be more than 150mV lower than the ground, nor shall it be connected with a transient bias, otherwise, problems may occur when the power supply is powered on or off. In order to ensure the voltage driving any input pin, no voltage faster than the voltage of CBM 08AD1500 power supply pin can appear at the analog or digital input terminal.

The absolute maximum rating shall be strictly observed even during power on and power off. When the power supply is turned on or off, a voltage spike will be generated to damage the CBM08AD1500. Figure 14 provides a power supply overshoot protection circuit.

In addition to a minimum load supply, many regulators provide power on output spikes, and active devices absorb very small currents, which can reach hundreds of millivolts. This result is a power on spike, which can damage the CBM08AD1500 unless the power supply is the minimum load. To ensure that there is no power on spike, connect a 100 Ω resistor at the output terminal of the regulator to provide a minimum output current during power on. In Figure 14, if the power supply voltage is 4V ~ 5V, a CBM317 linear regulator can meet the requirements; If a

3.3V power supply is used, the CBM1764 linear regulator is recommended. The output drive has a power supply voltage V_{DD}, which should be within the specified range of the working rating. This voltage should not exceed the analog power supply voltage VCC, and its voltage spike should never exceed V_{CC}+100mV. After the device is powered on, if there is no clock signal input, the current of the device may be less than 200mA. This is because the CBM08AD1500 reset is controlled by clock logic, so its initial state is unknown. If the reset logic comes in the "on" state, it will cause most analog circuits to enter the power down mode, so that the power supply current does not exceed 100mA. This current is greater than the current in the power-saving mode, because not all parts of the ADC are in the power-saving state, and the device current will be normal after the input clock is established.

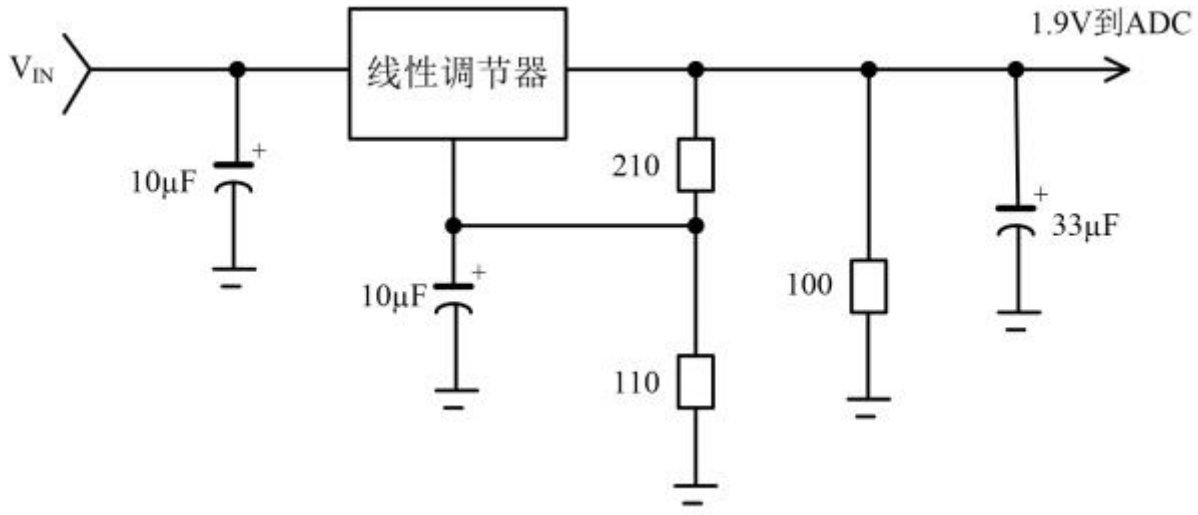


Figure 14. Power supply without peak

b. Heat treatment

For the CBM08AD1500 with such ultra-high speed and high performance, the power consumption is very low. However, in terms of pure power consumption, it is still very large, and attention should be paid to its heat treatment. For reliability reasons, the maximum temperature of the chip should not exceed 150 ℃. That is to say, T_A (ambient temperature) plus

ADC power consumption times θ_{JA} (junction to ambient thermal resistance) shall not exceed 150 ℃. As a convenience for users, the CBM08AD1500 contains a thermal diode for temperature measurement. But the characteristics of thermal diode

No characterization, and the process did not provide accurate information. Please note that it is recommended to install components on PCB. The starting point on the PCB and the development assembly process should be considered. It is recommended to follow the experience of packaging and installation in the past. There is a gold-plated pad at the bottom of the CBM08AD1500 package, which provides a main heat dissipation channel and has a very good grounding effect to the printed circuit board. The design of the lead pattern welded to the PCB is the same as the common CQFP, but the bottom gold-plated pad of the package must be welded to the PCB to remove the heat on the package to the maximum extent and ensure the best product performance. In order to remove the heat on the package to the greatest extent, a thermal connection pattern in the package area must be embedded on the PC board. The bottom of the device must be welded until sufficient heat conduction is ensured outside the package area. The lead pattern design of this exposed pad should be the same size as the bottom of the package, with a size of 14.1 × 14.1mm2, located at the bottom of the device, and completely covered with the hot lead pattern, which shall be connected to the ground.

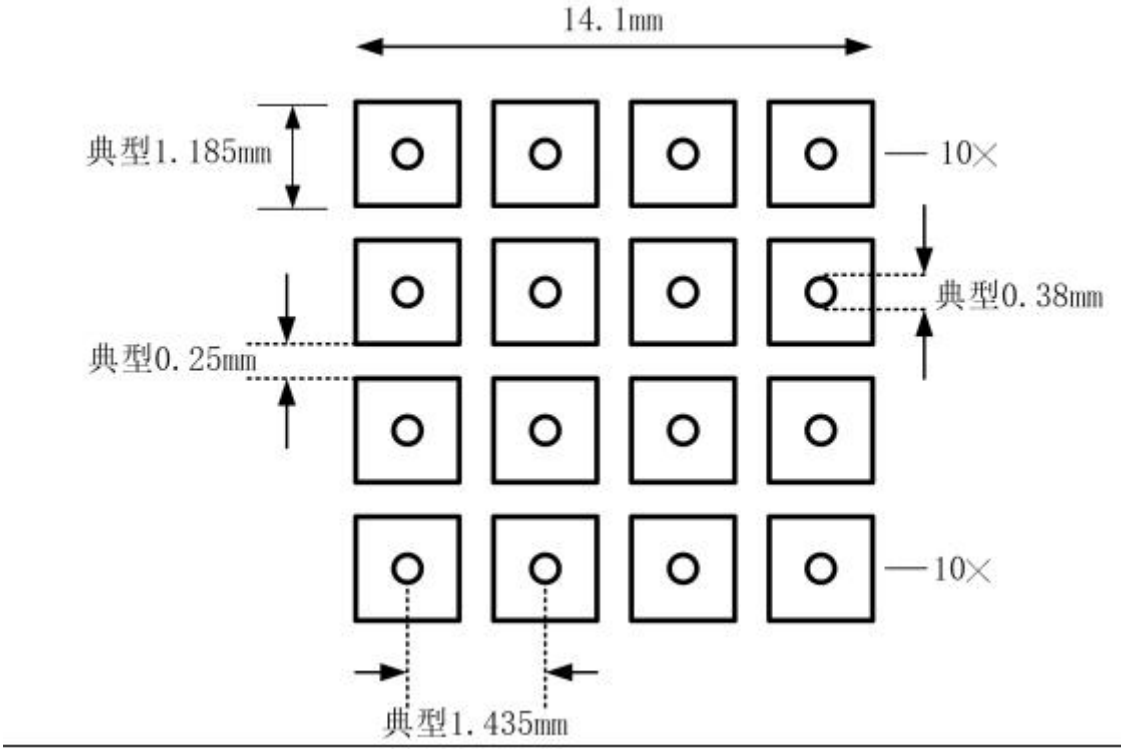


Figure 15. Recommended Packaging Connection Graph

As a large hole opening may lead to poor contact, the hole opening should be subdivided into a small hole array, similar to the connection figure in Figure 15. To minimize the junction temperature, it is recommended to install a simple heat sink on the PCB. This is to make a copper area of about 14.5 square centimeters on the opposite side of the PCB. This copper area can be gold-plated or coated with a layer of solder to prevent corrosion, but there should be no conformal coating, which may provide some thermal insulation. Hot holes should be used to connect the top and bottom copper areas. These hot holes play the role of "heat pipes", transferring heat energy from one side of the PCB to the opposite side, which is conducive to more effective heat release. It is recommended to use nearly 100 hot holes. The typical distance between these hot holes is 1.435mm, and the typical diameter of the holes is 0.38mm. These holes should be a cylinder with gold plating to prevent welding materials from falling into the holes during welding, because these welding materials will form pores between PCB and package exposed pads. These pores will increase the thermal resistance between the device and the hot pad on the board, which will cause the device to work hot. If you want to monitor the chip temperature, the temperature sensor is installed in the heat sink area near the hot hole on the board. Consider that the thermal gradient between the temperature sensor and the CBM08AD1500 chip is equal to θ J-PAD × Typical power consumption (2.0 × 2.2=4.4 ℃), considering 6 ℃, including some allowance for the temperature difference from the pad to the temperature sensor, it will mean that the maximum pad temperature is 144 ℃, ensuring that the chip temperature does not exceed 150 ℃. Suppose that the exposed pads of the CBM 08AD1500 are properly welded, and there are enough hot holes. See Table 16 for package thermal resistance.

Package	**θ_{JA} (to the environment)**	**θ_{JC} (top to package)**	**$\theta_{J\text{-}PAD}$ (Thermal pad)**
CQFP128	13.5℃/W	3.8℃/W	2.0℃/W

Figure. 16 Thermal resistance of package

7) . Layout and grounding

Proper grounding and all signal wiring fundamentally ensure correct conversion, and a single ground plane should be used instead of the ground plane separating analog and digital areas. Because the digital switching transient is composed of a large number of high-frequency components, the surface effect tells us that the noise generated by the logic of a whole ground plane has little impact, and the total surface area is more important than the total ground plane

volume. The coupling between a typical noisy digital circuit and a sensitive analog circuit leads to poor performance, which is impossible to isolate and repair. The solution is to separate the analog circuit from the digital circuit. High power digital parts cannot be located on or adjacent to these parts, which are: any linear element, power path, plane used for analog or mixed signals. Because these common loop current paths will cause the analog input ground back to ADC to fluctuate, causing additional noise to the conversion results. In order to avoid digital noise entering the analog channel, analog signal lines and digital signal lines are usually crossed at 90 ° with each other. However, in the high-frequency system, the analog signal line and the digital signal line should not be completely crossed, and the input clock signal line should be isolated from all analog and digital lines. It is generally recognized that the 90 ° crossing should be avoided, because even a little bit of coupling will cause problems in the high-frequency system. Therefore, the best performance will be obtained by using the linear signal path in the high-frequency system. The analog input should be isolated from the noise signal path to avoid pseudo signal coupling to the input, which is particularly important when the CBM08AD1500 is driven by low-level signals. Any external components (such as filter capacitors) connected between the input of the converter and the ground shall be connected to a very clean point on the analog ground plane, and all analog circuits (input amplifiers, filters, etc.) shall be isolated from any digital components.

8) . Dynamic performance

The CBM08AD1500 is AC tested, and its dynamic performance is guaranteed. In order to meet the technical requirements and avoid noise introduced by jitter, the clock source driving the INCLK input must have low root mean square jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in 2.3).

In practical applications, it is a good habit to make the ADC input clock line as short as possible, keep it far enough away from any other signal line, and regard it as a transmission line. Other signal lines may introduce jitter to the input clock signal. If they are not separated from these paths, the clock signal can also introduce noise to the analog path. The best dynamic performance is achieved when the exposed pads on the back of the package are well connected to the ground. This is because the path from the chip to the ground is low resistance, which is lower than the path provided by the package pin.

9) . Serial interface use

CBM08AD1500 may work in non extended control mode (without serial interface) or extended control mode. Table 17 and Table 18 describe the functions of pins 3, 4, 14 and 127 in non extended control mode and extended control mode respectively.

a. Normal (non extended) control mode operation

The common control mode means that the serial interface is invalid and all control functions are controlled by various pin pin settings, namely, the full scale range, power on correction delay, output voltage and input coupling (a.c or d.c). The non extended control mode is selected by setting pin pin 14 to high or low. Instead, it is suspended.

PIN	Low level	High level	suspend
3	Reduced output amplitude	Normal output amplitude	Normal output amplitude
4	Bottom edge of output clock	Upper edge of output clock	DDR Mode
127	Short power on delay	Long power on delay	No use
14	Reduced input amplitude	Normal input amplitude	Extended Control Mode

Table 17. Common control mode (pin 14 is high or low)

In extended control mode: Pin pin 3 can also be high or low; Pin pin 14 must be suspended or $V_{CC}/2$; For more information, see 1.2) General/Extended Control. Pin 4 can be high, low or suspended in normal control mode; In the normal control mode, pin 4 high or low defines that the output data is converted on the other side of the output clock. For more information, see 2.4) C Output edge synchronization. If pin 4 of this pin is suspended, the output clock (Q_{CLK}) is a DDR (dual data rate) clock (see 1.1). e. ③ Dual data rate). Since data is output at both edges of the Q_{CLK}, the data output is not synchronized with the output clock. Pin 127 sets the correction delay in the normal control mode, and pin 127 cannot be suspended.

PIN	Function
3	SCLK (Serial Clock)
4	DATA(Serial Data)
127	$\overline{ST2}$ (Serial interface strobe)

Table 18. Extended control mode (pin 14 suspended or $V_{CC}/2$)

10) . Mistakes easily made in general application

For the reliability of the device, the drive input (analog or digital) shall not be far away from the power supply voltage. Any input should not be 150mV lower than the ground pin or 150mV higher than the power supply voltage pin. Even the transient bias should not exceed these limits. Otherwise, it will not only change the device performance, but also reduce the reliability of the device. It is also not possible for high-speed digital circuits to overshoot below the ground. In their characteristic impedance, the impedance control of high-speed lines and the impedance of the terminals of these lines should control their overshoot. It should be noted that the input drive of the CBM08AD1500 should not be over pressured, otherwise it will lead to incorrect conversion, or even damage the components. Wrong analog input common mode voltage in DC coupling mode. E.g. 1.1) D Analog input and 2.2) Analog input describe that the input common mode voltage must be kept within 50mV of V_{CMO} output, and the change with temperature must be tracked. If the input common mode voltage exceeds VCMO ± 50mV, the performance will be degraded.

Drive the analog input with an inappropriate amplifier. Be careful when selecting a high-speed amplifier to drive the CBM08AD1500, because many high-speed amplifiers have higher distortion than the CBM08AD1500, which will lead to the degradation of the overall system performance.

Overdriving the V_{REF} pin will change the reference voltage. As mentioned in 2.1) Reference voltage, the reference voltage is set through the FSR pin fixed or full scale voltage regulation register. Overdriving this pin will not change the full scale value, but will cause the device to work abnormally.

Drive the clock input with a very high voltage signal. ADC clock input level shall not exceed the level described in the recommended operating conditions, and the input bias shall not be changed.

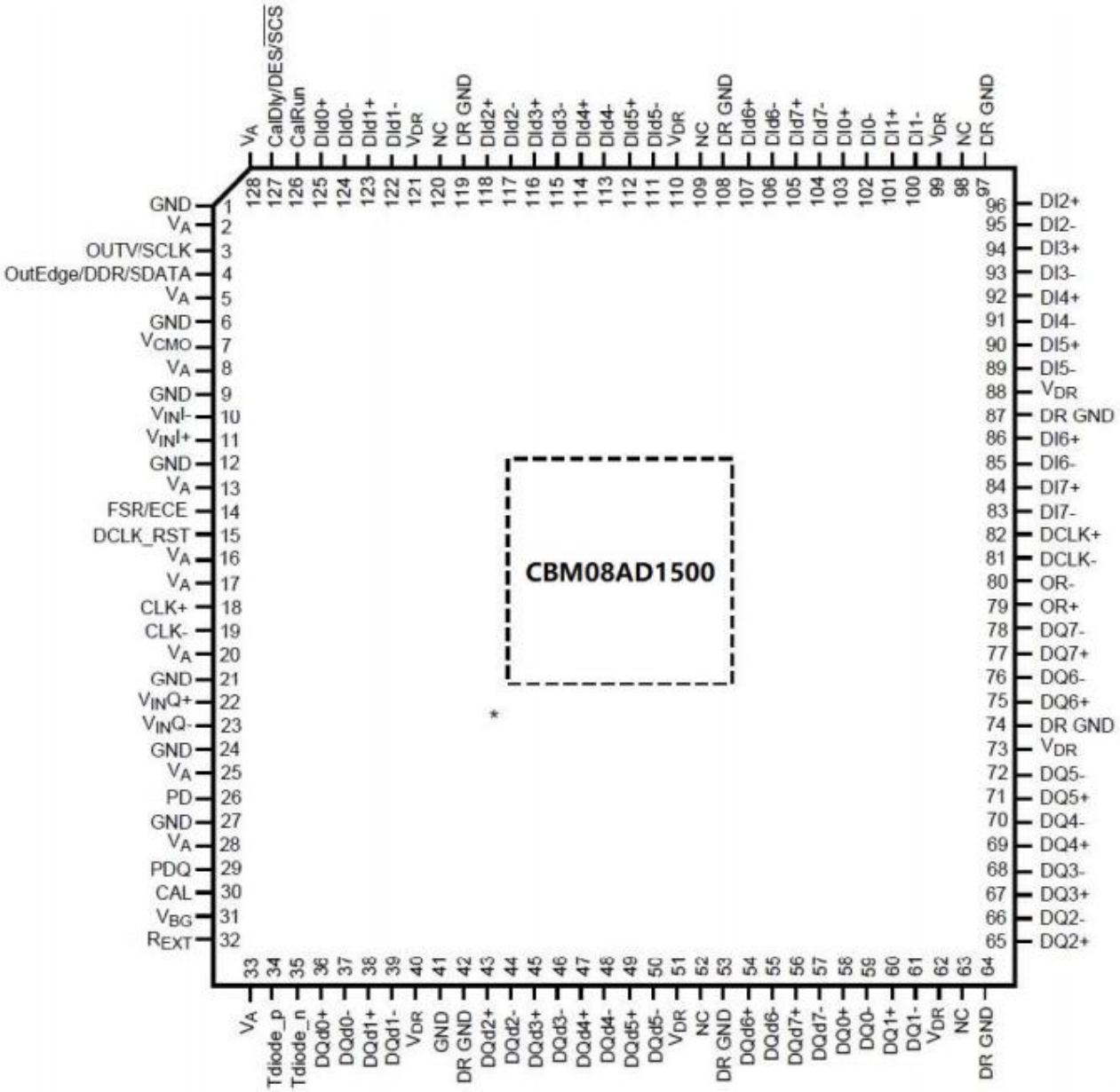
Improper clock input level. As described in 2.3) Clock input, too low clock input level will lead to poor performance, and too high clock input level will lead to input offset.

Use a clock source with excessive jitter, use a very long input clock signal path, or have other signals coupled to the input clock signal line. This will cause the sampling interval to change, resulting in excessive output noise and reducing SNR performance.

Insufficient heat dissipation. E.g. 2.6) B As described in heat treatment, it is important to provide sufficient heat dissipation to ensure the reliability of devices, which can be achieved by

sufficient air flow or by using a simple heat dissipation device placed on the board. For best performance, the bonding pad on the back should be grounded.

Pin configuration diagram



Pin description

Pin Number	Symbol	Pin Description	Pin Number	Symbol	Pin Description
1	GND_D	Analog ground	65	D_{Q2}	Q channel data output bit D_{Q2}
2	V_{CC}	Analog Supply	66	D_{Q2}	Q channel data output bit DQ2
3	Outv/SCLK	Output voltage amplitude control/serial interface clock input	67	D_{Q3}	Q channel data output bit D_{Q3}
4	OutEdge / DDR/DATA	Output clock edge selection/dual data rate control/serial data input	68	D_{Q3}	Q channel data output bit D_{Q3}
5	V_{CC}	Analog Supply	69	D_{Q4}	Q channel data output bit D_{Q4}
6	GND_A	Analog ground	70	D_{Q4}	Q channel data output bit D_{Q4}
7	V_{CMO}	Common mode voltage	71	D_{Q5}	Q channel data output bit D_{Q5}
8	V_{CC}	Analog Supply	72	D_{Q5}	Q channel data output bit D_{Q5}
9	GND_A	Analog ground	73	V_{DD}	Output drive power
10	IN_{I-}	I channel analog input negative	74	GND_D	Output drive ground
11	IN_{I+}	I channel analog input positive	75	D_{Q6}	Q channel data output bit D_{Q6}
12	GND_A	Analog ground	76	D_{Q6}	Q channel data output bit D_{Q6}
13	V_{CC}	Analog Supply	77	D_{Q7}	Q channel data output bit D_{Q7} (Highest bits)
14	FSR/ST1	Full scale range selection/extended control mode selection	78	D_{Q7}	Q channel data output bit D_{Q7} (Highest bits)
15	R	Clock set control input	79	DOR	Overflow in-phase output

16	V_{CC}	Analog Supply	80	DOR	Overflow inverted output
17	V_{CC}	Analog Supply	81	QCLK	Data clock inverted output
18	INCLK+	Clock input positive	82	QCLK	Data clock in-phase output
19	INCLK-	Clock input negative	83	DI7	I channel data output bit D_{I7} (Highest bits)
20	V_{CC}	Analog Supply	84	DI7	I channel data output bit D_{I7} (Highest bits)
21	GND_A	Analog ground	85	DI6	I channel data output bit D_{I6}
22	IN_{Q+}	Q channel analog input positive	86	DI6	I channel data output bit D_{I6}
23	IN_{Q-}	Q channel analog input negative	87	GND_D	Output drive ground
24	GND_A	Analog ground	88	VDD	Output drive power
25	V_{CC}	Analog Supply	89	DI5	I channel data output bit D_{I5}
26	PD	Power saving mode control	90	DI5	I channel data output bit D_{I5}
27	GND_A	Analog ground	91	DI4	I channel data output bit D_{I4}
28	V_{CC}	Analog Supply	92	DI4	I channel data output bit D_{I4}
29	PDQ	Q channel Power saving mode control	93	DI3	I channel data output bit D_{I3}
30	CAL	Correction control	94	DI3	I channel data output bit D_{I3}
31	VREF	Reference output	95	DI2	I channel data output bit D_{I2}
32	Rext	External resistance	96	DI2	I channel data output bit D_{I2}
33	V_{CC}	Analog Supply	97	GND_D	Output drive ground
34	Tdiode_p	Temperature diode positive	98	NC	Not connect
35	Tdiode_n	Temperature diode negative	99	VDD	Output drive power

36	DQd0	Q channel data output bit D_{QD0} (Lowest bits)	100	DI1	I channel data output bit D_{I1}
37	DQd0	Q channel data output bit D_{QD0} (Lowest bits)	101	DI1	I channel data output bit D_{I1}
38	DQd1	Q channel data output bit D_{QD1}	102	DI0	I channel data output bit D_{I0} (Lowest bits)
39	DQd1	Q channel data output bit D_{QD1}	103	DI0	I channel data output bit D_{I0} (Lowest bits)
40	VDD	Output drive power	104	DID7	I channel data output bit D_{ID7} (Highest bits)
41	GND_A	Analog ground	105	DID7	I channel data output bit D_{ID7} (Highest bits)
42	GND_D	Output drive ground	106	DID6	I channel data output bit D_{ID6}
43	DQd2	Q channel data output bit D_{QD2}	107	DID6	I channel data output bit D_{ID6}
44	DQd2	Q channel data output bit D_{QD2}	108	GND_D	Output drive ground
45	DQd3	Q channel data output bit D_{QD3}	109	NC	Not connect
46	DQd3	Q channel data output bit D_{QD3}	110	VDD	Output drive power
47	DQd4	Q channel data output bit D_{QD4}	111	DID5	I channel data output bit D_{ID5}
48	DQd4	Q channel data output bit D_{QD4}	112	DID5	I channel data output bit D_{ID5}
49	DQd5	Q channel data output bit D_{QD5}	113	DID4	I channel data output bit D_{ID4}
50	DQd5	Q channel data output bit D_{QD5}	114	DID4	I channel data output bit D_{ID4}
51	VDD	Output drive power	115	DID3	I channel data output bit D_{ID3}
52	NC	Not connect	116	DID3	I channel data output bit D_{ID3}
53	GND_D	Output drive ground	117	DID2	I channel data output bit D_{ID2}

54	DQd6	Q channel data output bit D_{QD6}	118	DID2	I channel data output bit D_{ID2}
55	DQd6	Q channel data output bit D_{QD6}	119	GND_D	Output drive ground
56	DQd7	Q channel data output bit D_{QD7} (Highest bits)	120	NC	Not connect
57	DQd7	Q channel data output bit D_{QD7} (Highest bits)	121	VDD	Output drive power
58	DQ0	Q channel data output bit D_{QD0} (Lowest bits)	122	DID1	I channel data output bit D_{ID1}
59	DQ0	Q channel data output bit D_{QD0} (Lowest bits)	123	DID1	I channel data output bit D_{ID1}
60	DQ1	Q channel data output bit D_{I1}	124	DID0	I channel data output bit D_{ID0}
61	DQ1	Q channel data output bit D_{I1}	125	DID0	I channel data output bit D_{ID0}
62	VDD	Output drive power	126	QCAL	Correction operation indication output
63	NC	Not connect	127	CalDly /DES /ST2	Power on correction delay selection/double edge sampling control/serial interface strobe
64	GND_D	Output drive ground	128	V_{CC}	Analog Supply

Matters needing attention

1. The external resistance Rext of pin 32 must be exactly equal to 3.3kΩ ± 0.1%, and other values cannot be used, as described in 1.1). a.
2. In application, it is recommended that PCB be grounded in large area. This can eliminate the potential difference due to different grounding points, and reduce the influence of capacitance generated by the circuit board on the circuit.
3. When using, do not insert the circuit reversely, otherwise the circuit may be damaged.
4. Each power supply pin needs to be connected to a nearest 0.1 μ F and 33 μ F capacitance.

5. The routing of differential analog input must be equal.

6. The digital power supply and the analog power supply need to be separated.

7. All leading out ends of the circuit are designed with electrostatic protection structure, but large energy electric pulse may still damage the circuit, so pay attention to electrostatic protection during testing, handling and storage.